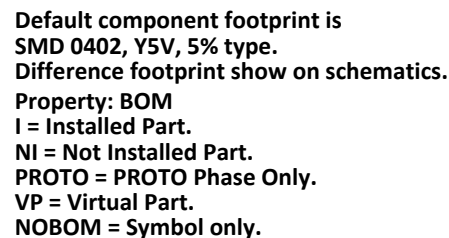


Monster (Shark Bay) Revision A00_2013/05/20

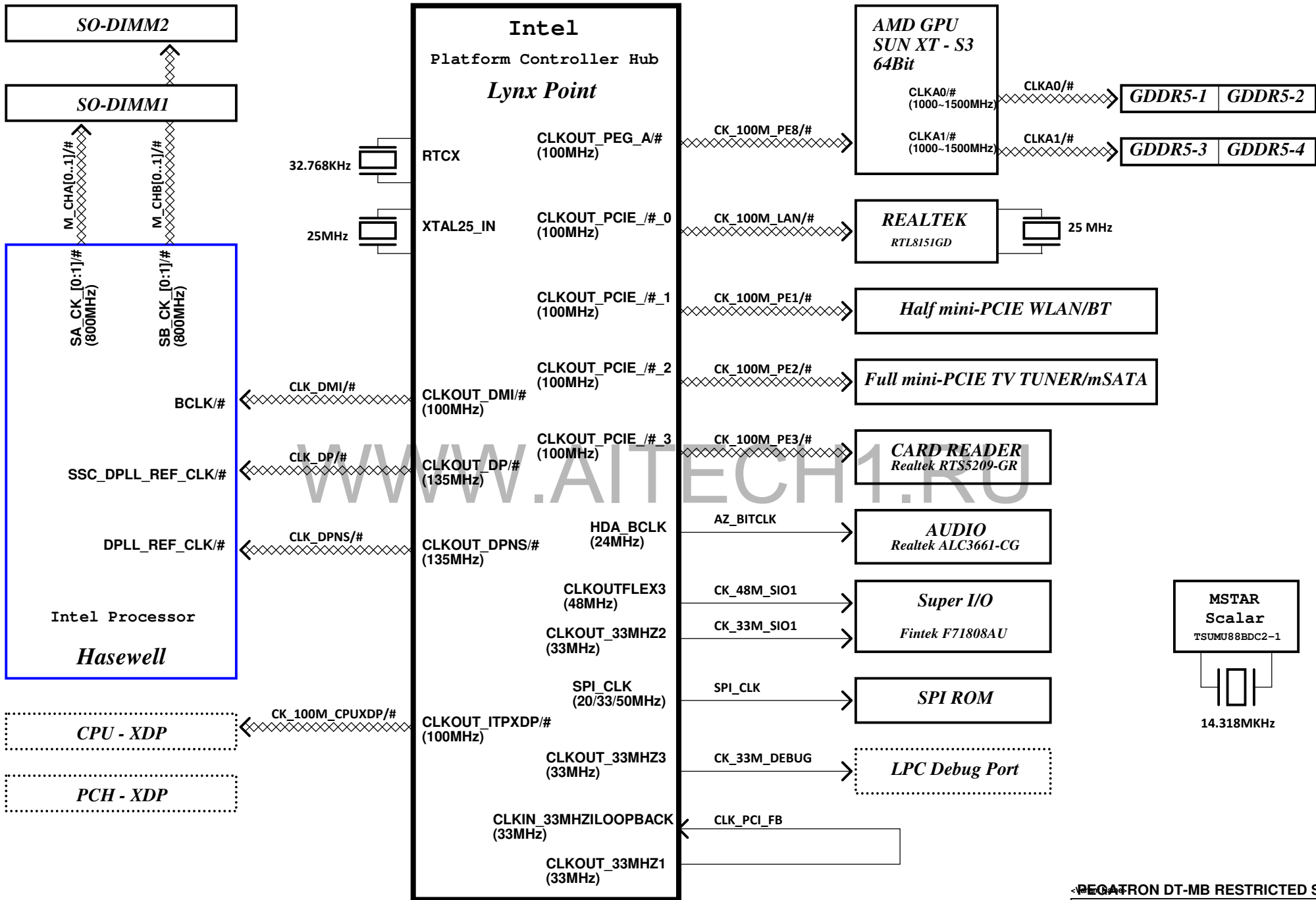
71	+1P35V GPU & +VDDCI
72	+VDDC controller
73	+VDDC CAP
74	+1P2V & +1P05V PCH
75	+3VA / 5VA / 3VSB / 5VSB
76	VCORE CONTROLLER
77	VCORE DRIVER 2-1
78	VCORE DRIVER 2-2 & Cout
79	DISCHARGE
80	CARD USB3.0 X2

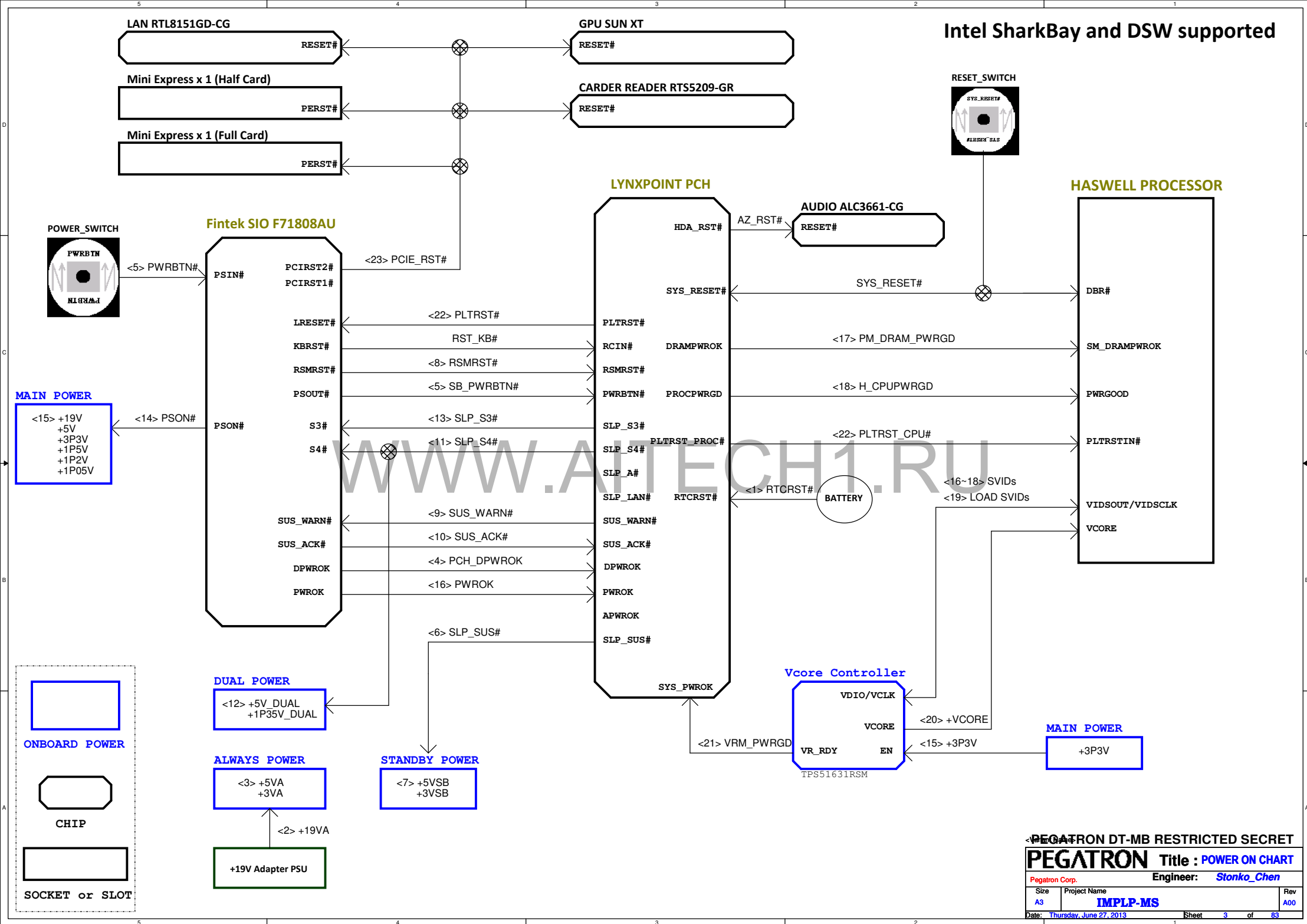


PEGATRON Title : **BLOCK DIAGRAM**

Size A3	Project Name IMPLP-MS	Rev A00
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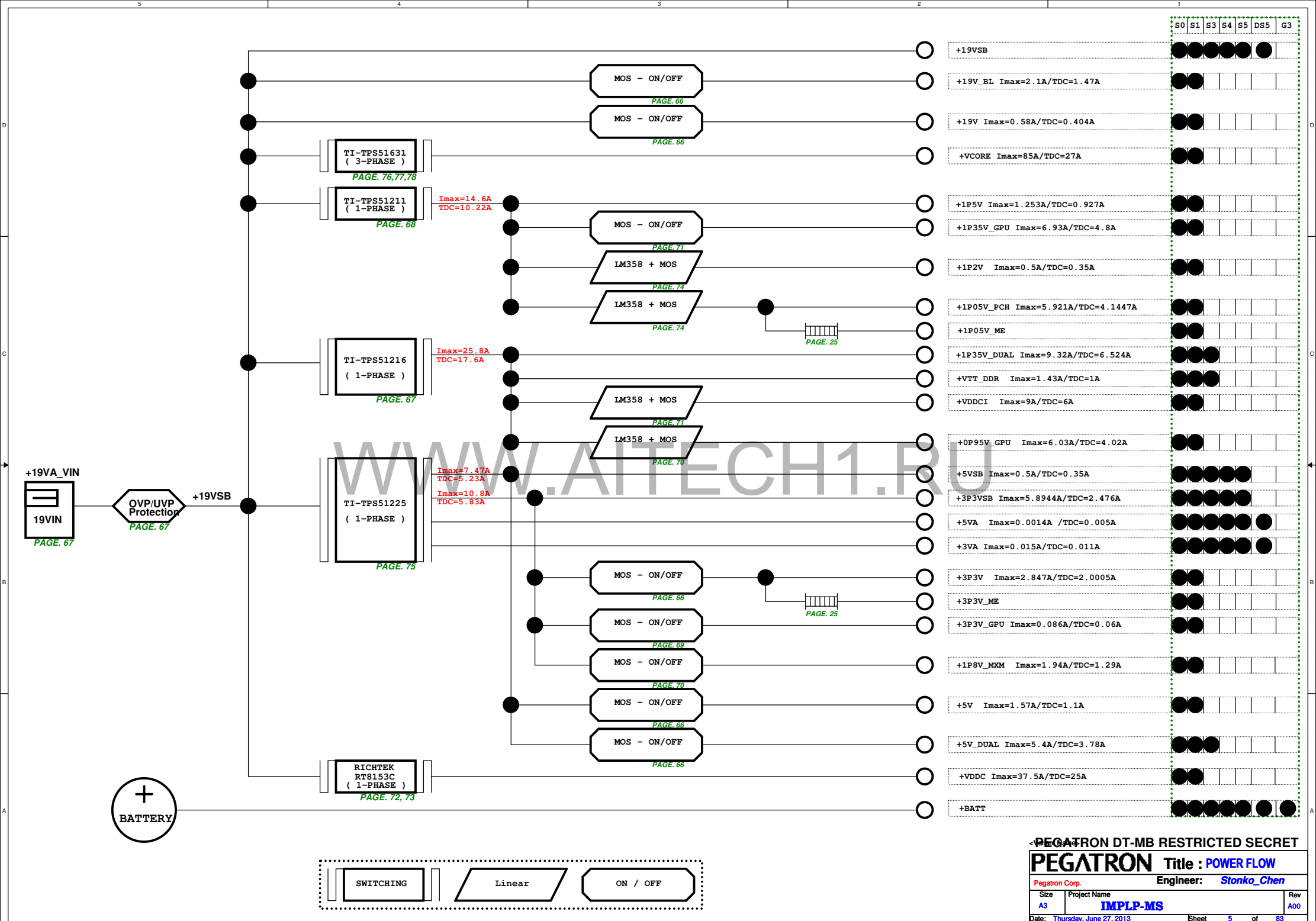
Date: Thursday, June 27, 2013 Sheet 1 of 83





Schematics Change History

[illegible]



Intel Haswell CPU			
	I (max) (A)	TDC (A)	Wattage (W)
+VCORE	85	27	47
+1P35V_DUAL	4.2	2.94	5.67

Intel PCH - Lynx Point HM87			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.202	0.141	0.67
+3P3VSB	0.293	0.205	0.97
+3VA	0.015	0.011	0.05
+1P5V	0.253	0.177	0.38
+1P05V_PCH	5.921	4.1447	6.22

AMD GPU - SUN-XT (64bit)			
	I (max) (A)	TDC (A)	Wattage (W)
+VDDC(1.125V)	37.5	25	49.19
+VDDCI(0.95V)	9	6	8.55
+3P3V_GPU	0.086	0.06	0.283
+1P8V_MXM	0.53	0.35	0.954
+1P35V_GPU	1.5	1	2.025
+0P95V_GPU	6.03	4.02	5.73

GDDR5 - 2GB			
	I (max) (A)	TDC (A)	Wattage (W)
+1P35V_GPU	5.43	3.8	7.33

SO - DIMM x 2 (DDR3L)			
	I (max) (A)	TDC (A)	Wattage (W)
+1P35V_DUAL	5.12	3.584	6.912
+VTT_DDR	1.43	1	0.97

Scalar - MSTAR TSUMU88BDC2-1			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.5	0.35	1.65
+1P2V	0.5	0.35	0.6

LOM - Realtek RTL8151GD			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3VSB	0.1	0.07	0.33

Audio - Realtek ALC3661-CG			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.071	0.05	0.236
+5VSB	0.5	0.35	2.5

Audio AMP - TPA3110D2PWPR			
	I (max) (A)	TDC (A)	Wattage (W)
+19V	0.58	0.404	11.97

SIO - Fintek F71808AU			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.011	0.008	0.38
+3P3VSB	0.0014	0.001	0.005
+5VA	0.0014	0.001	0.005

Card Reader - Realtek RTS5209-GR			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	1.71	1.2	5.66

SATA 3.0 (1-Port for 2.5" HDD)			
	I (max) (A)	TDC (A)	Wattage (W)
+5V	1.57	1.1	7.86

mini_PCIE (Half card)			
	I (max) (A)	TDC (A)	Wattage (W)
+1P5V	0.5	0.375	0.5
+3P3VSB	2.75	1.1	9.075

mini_PCIE (Full card)			
	I (max) (A)	TDC (A)	Wattage (W)
+1P5V	0.5	0.375	0.5
+3P3VSB	2.75	1.1	9.075

USB3.0 (6-Ports)			
	I (max) (A)	TDC (A)	Wattage (W)
+5V_DUAL	5.4	3.78	27

Webcam			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.323	0.226	1.065

Touch			
	I (max) (A)	TDC (A)	Wattage (W)
+5V_DUAL	1.57	1.1	7.86

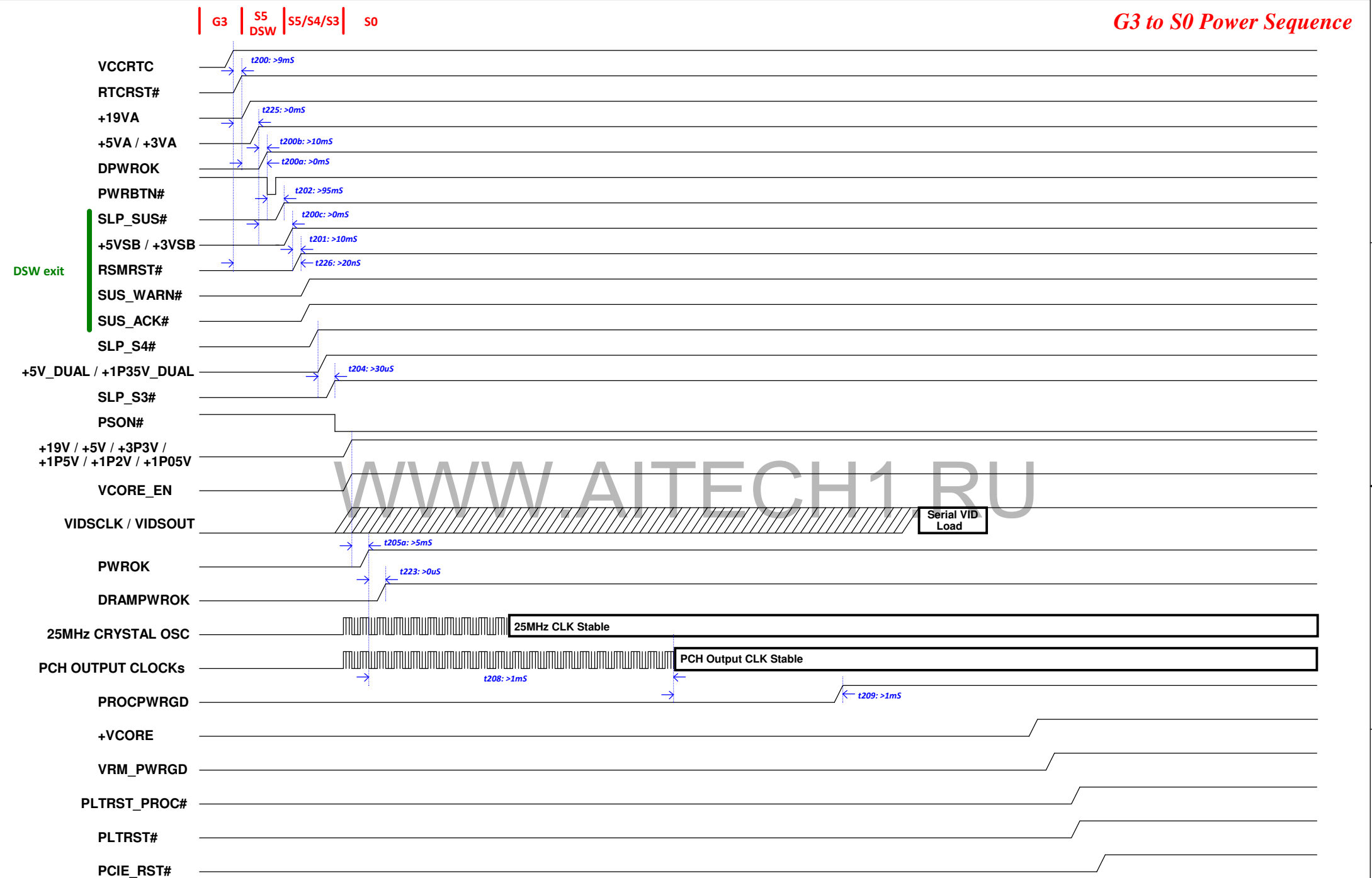
HDMI			
	I (max) (A)	TDC (A)	Wattage (W)
+5V	0.055	0.039	0.275

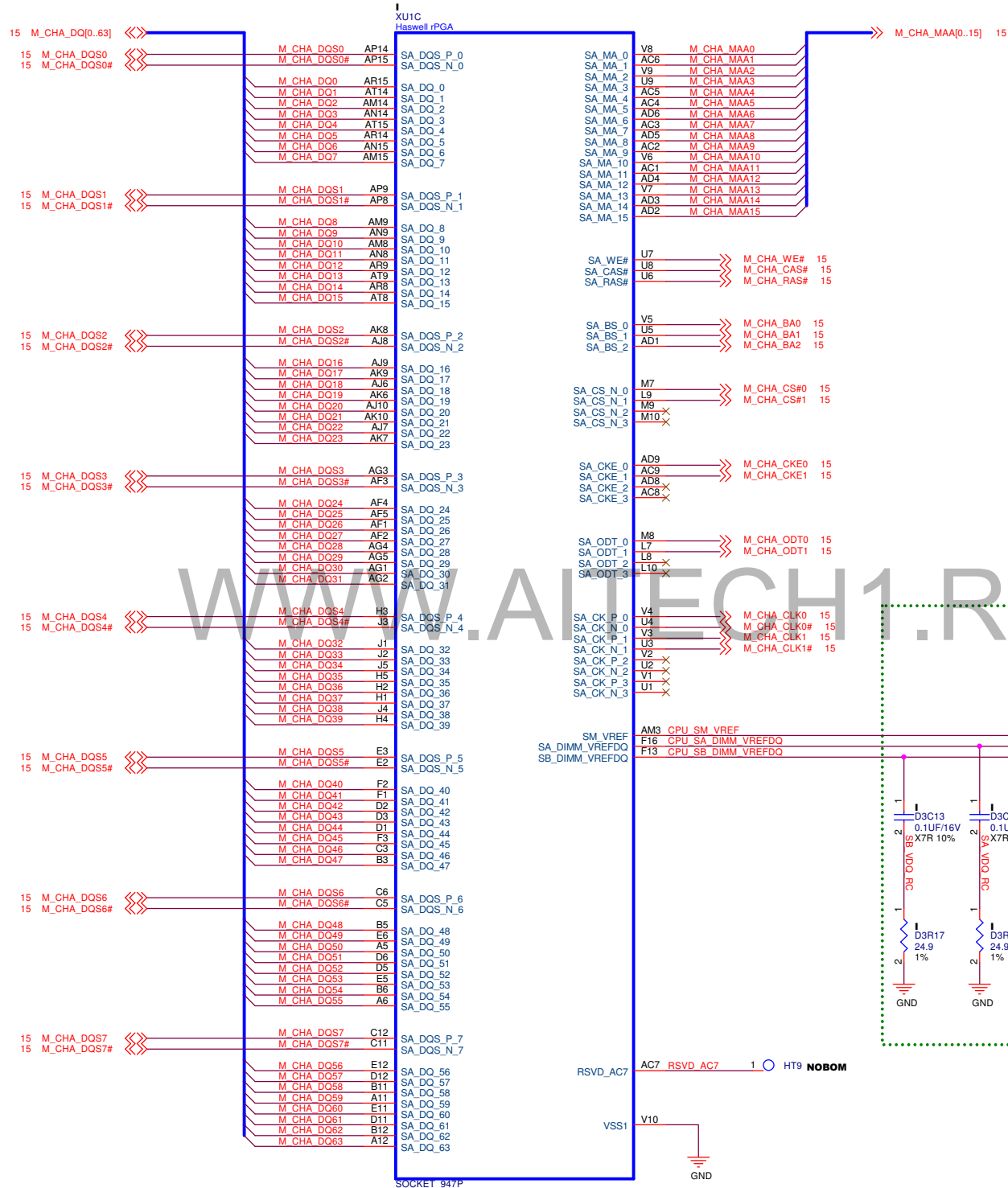
FAN			
	I (max) (A)	TDC (A)	Wattage (W)
+5V	0.5	0.35	2.5

SPI			
	I (max) (A)	TDC (A)	Wattage (W)
+3P3V	0.03	0.03	0.099

PANEL			
	I (max) (A)	TDC (A)	Wattage (W)
+19V_BL	2.1	1.47	39.9
+5V_LCD	1.1	0.8	0.5

G3 to S0 Power Sequence





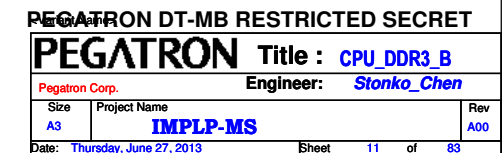
PEGATRON DT-MB RESTRICTED SECRET

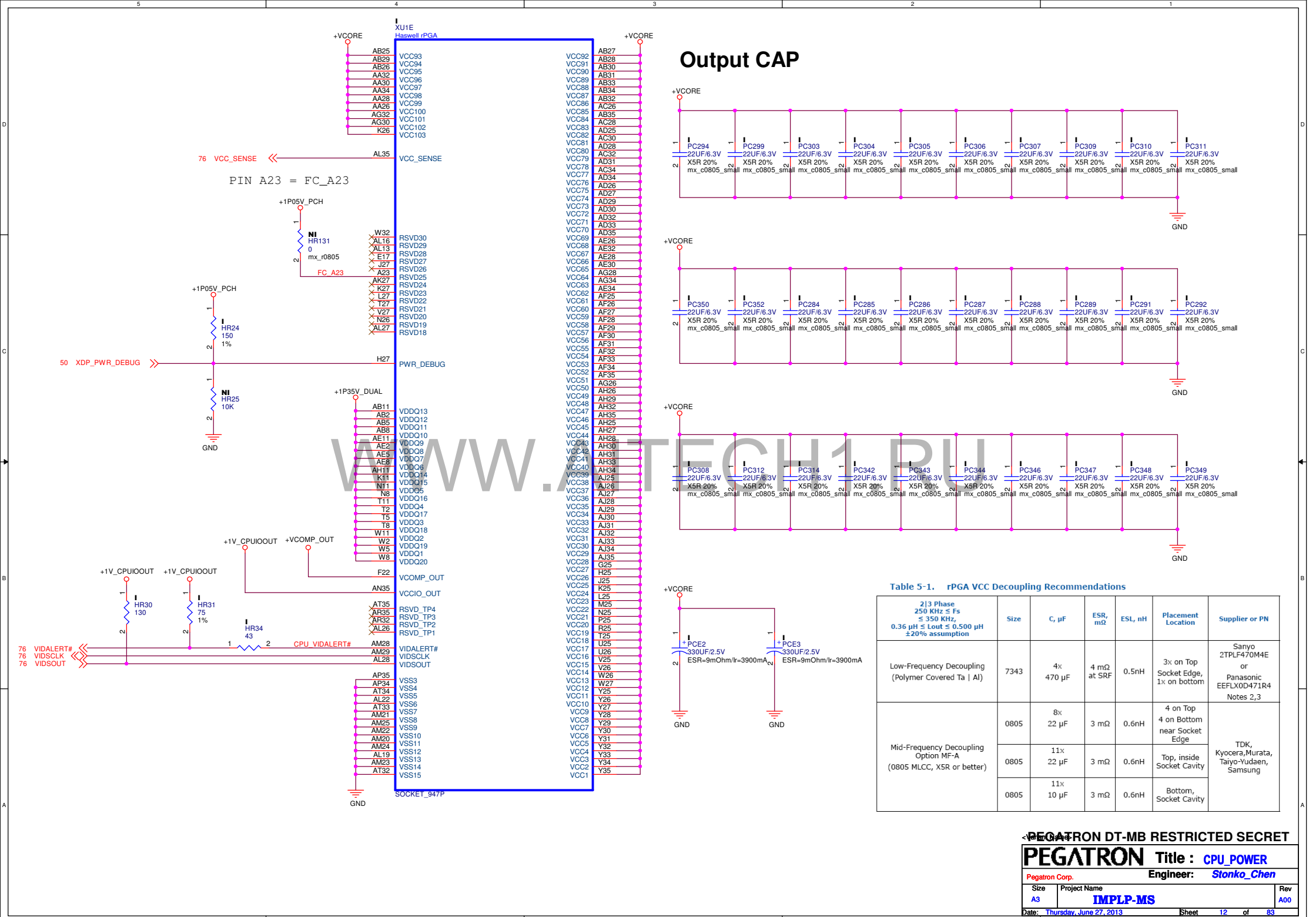
PEGATRON Title : CPU_DDR3_A

Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name IMPLP-MS Rev A00

Date: Thursday, June 27, 2013 Sheet 10 of 83





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU_POWER

Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00

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CFG[19:0] (default value of '1' if not terminated on the board.) [our setting = *]

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.

- 1 = Normal operation (*)
- 0 = Lane numbers reversed

CFG[3]: MSR Privacy Bit Feature

- 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting (*)
- 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

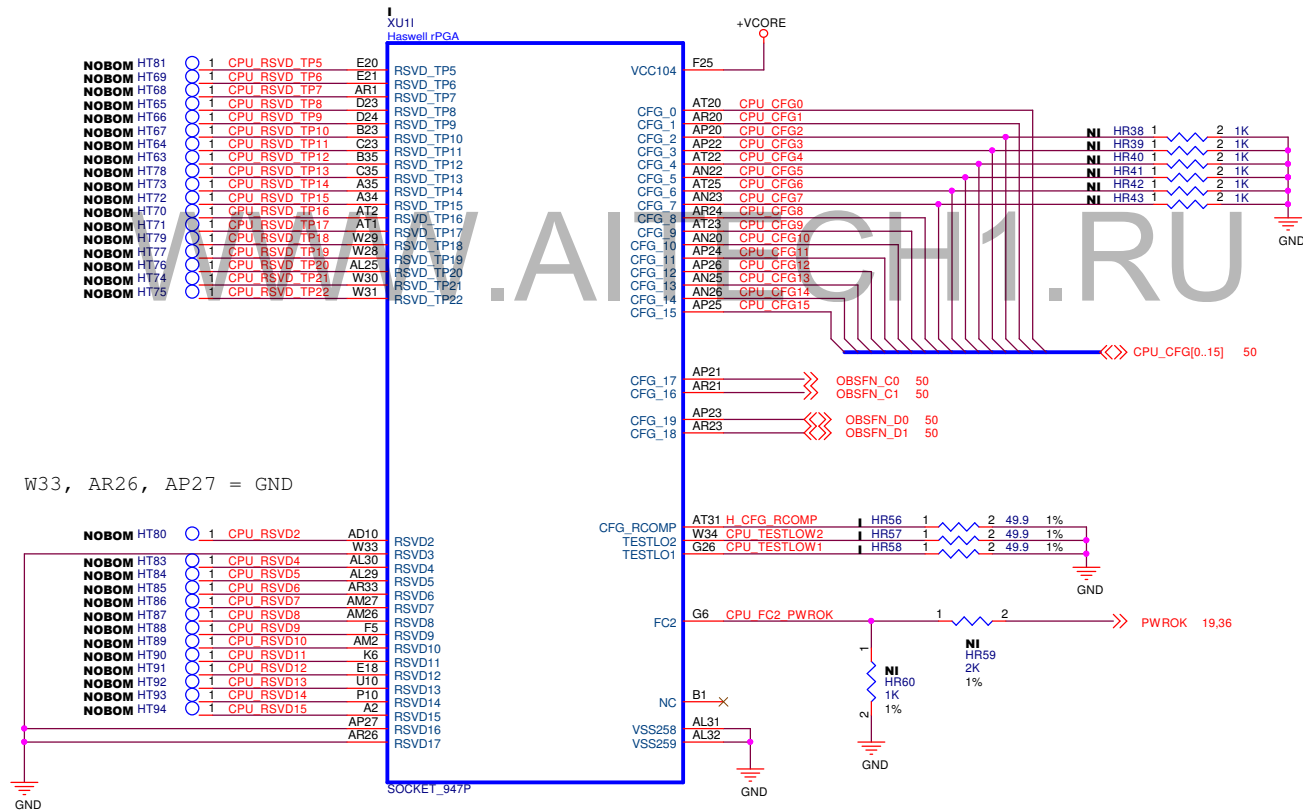
CFG[4]: eDP enable

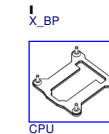
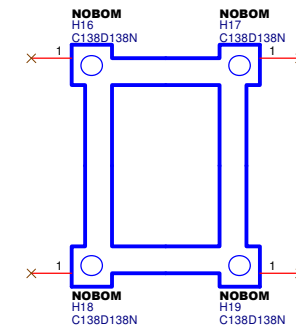
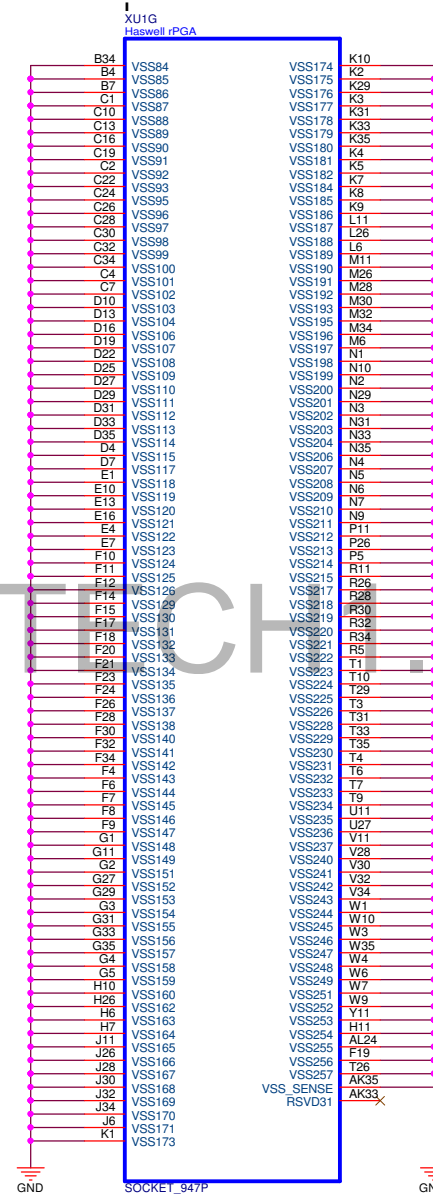
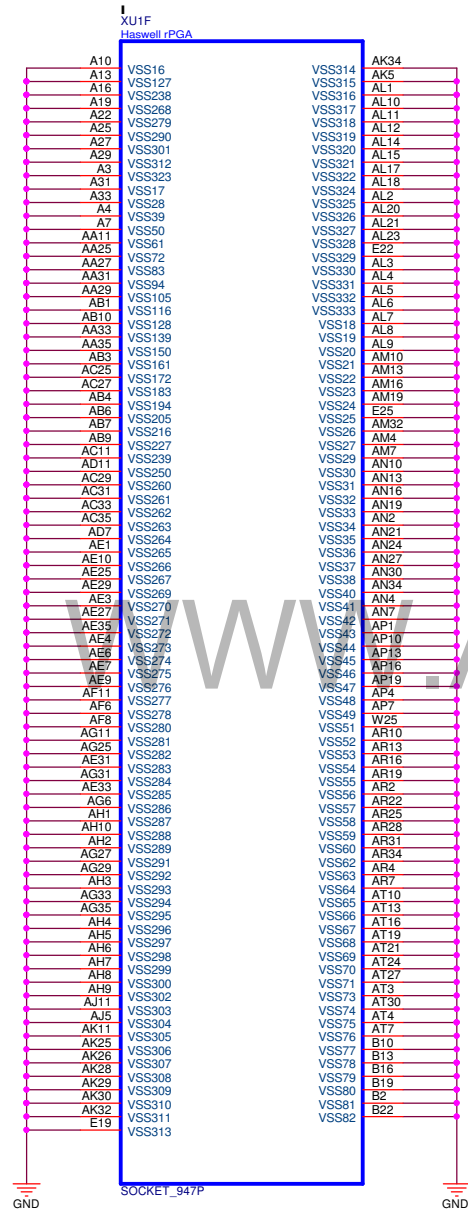
- 1 = Disabled (*)
- 0 = Enabled

CFG[6:5]: PCI Express* Bifurcation:

- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = 1 x16 PCI Express* (*)

CFG[1:0] ; CFG[19:7] Reserved configuration lanes. Need test point

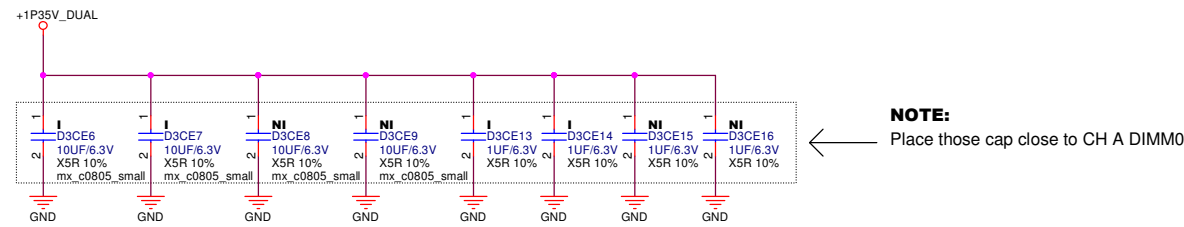




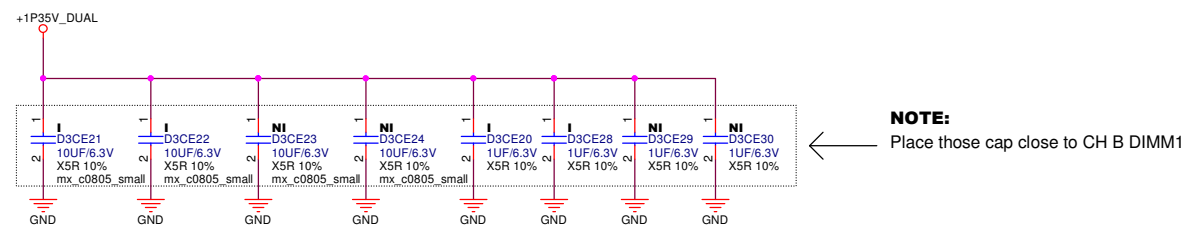
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CPU_GND	
Pegatron Corp.		Engineer: Stonko_Chen	
Size A3	Project Name IMPLP-MS	Rev A00	
Date: Thursday, June 27, 2013		Sheet 14 of 83	

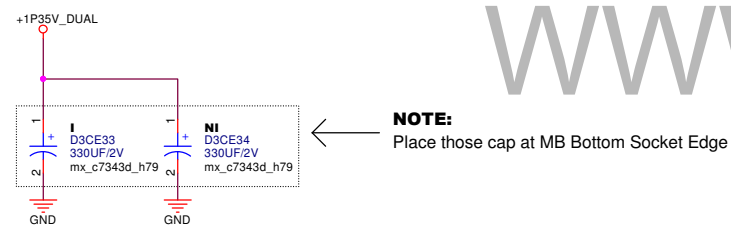
SO DIMM CHA DECOUPLING



SO DIMM CHB DECOUPLING

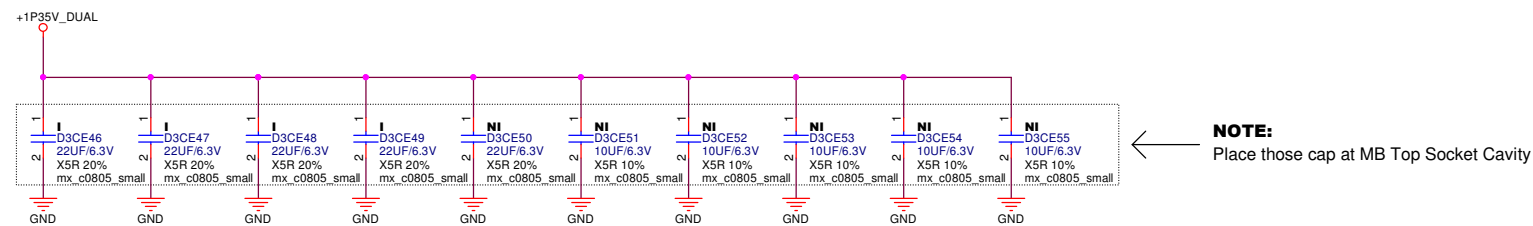
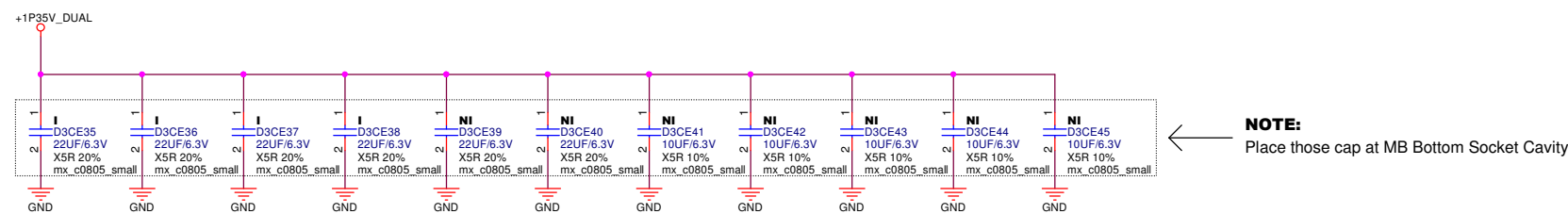


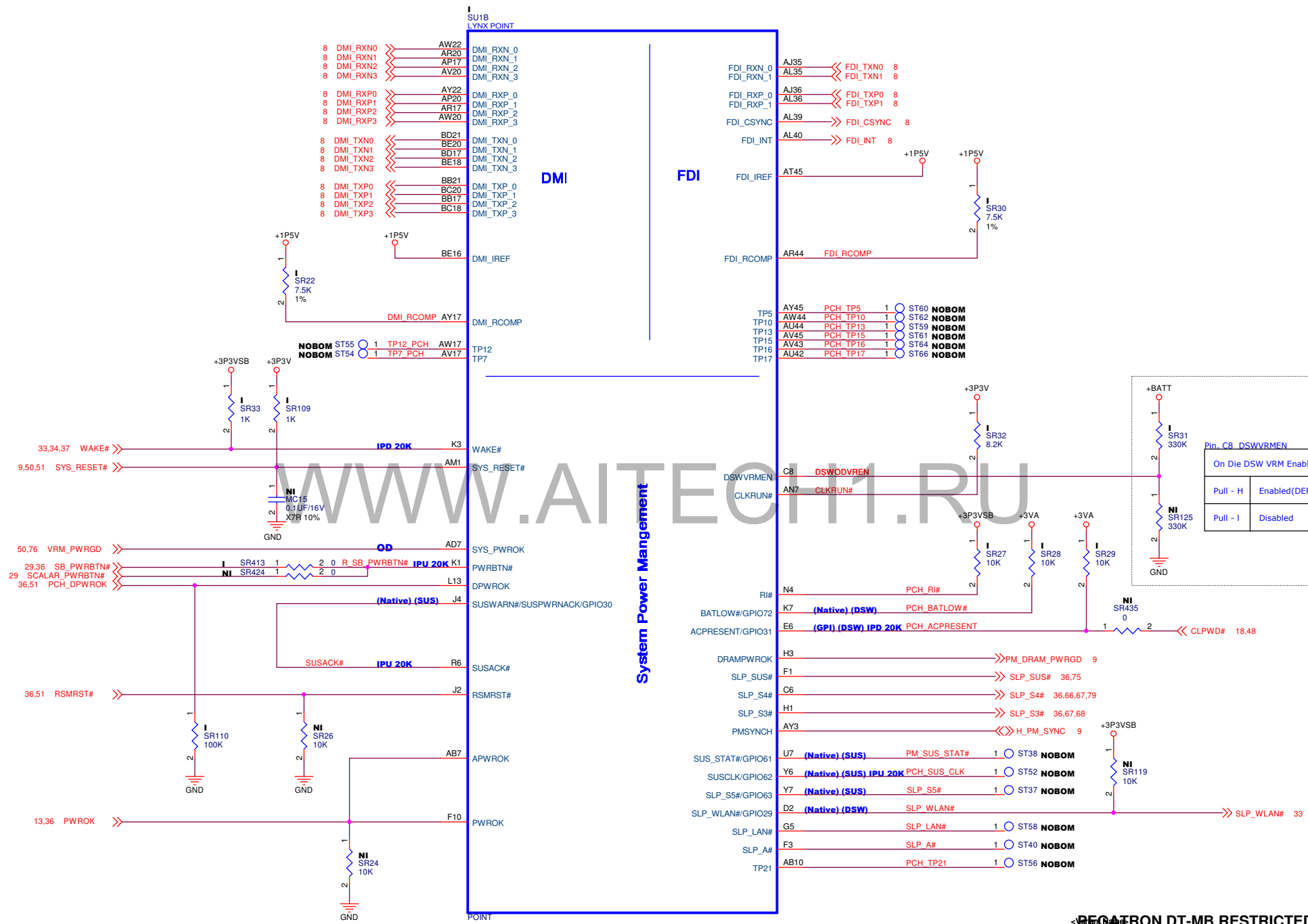
Processor VDDQ DECOUPLING

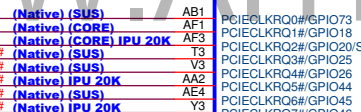
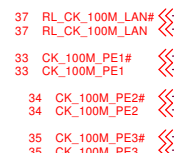


rPGA Processor VDDQ 1.5-V Rail Decoupling Location

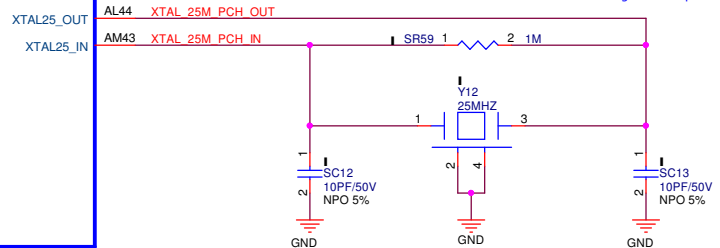
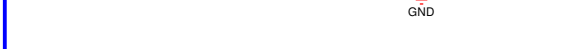
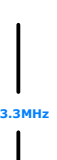
Bulk Decoupling Socket Edge	Qty x uF (size)	ESR
MB Bottom Socket Edge	2 x 330 uF	6 m Ohm
6x MB Bottom Socket Cavity	11 x 22 uF (0805)	3 m Ohm
5x MB Top Socket Cavity	10 x 10 uF (0805)	3 m Ohm



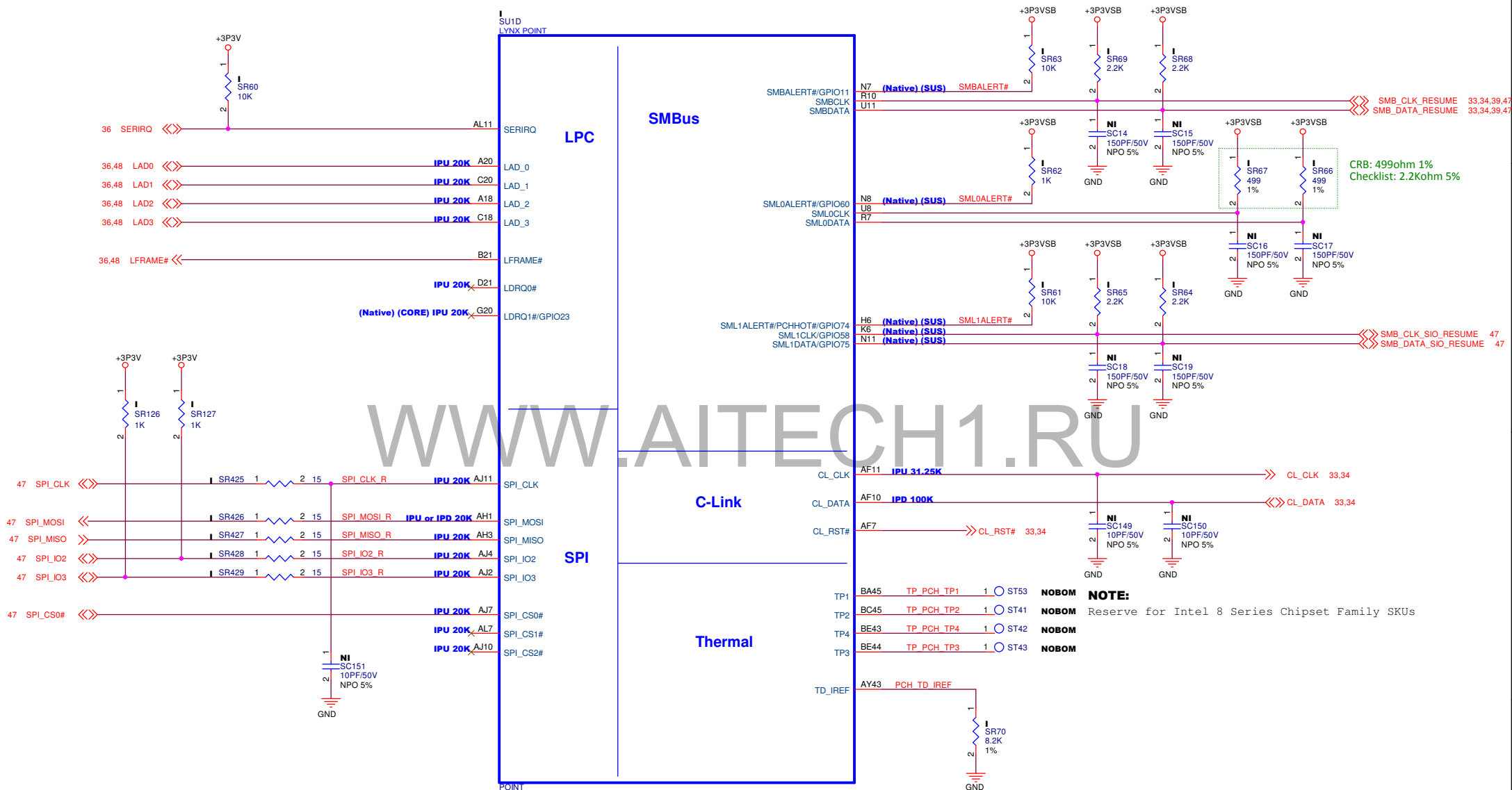


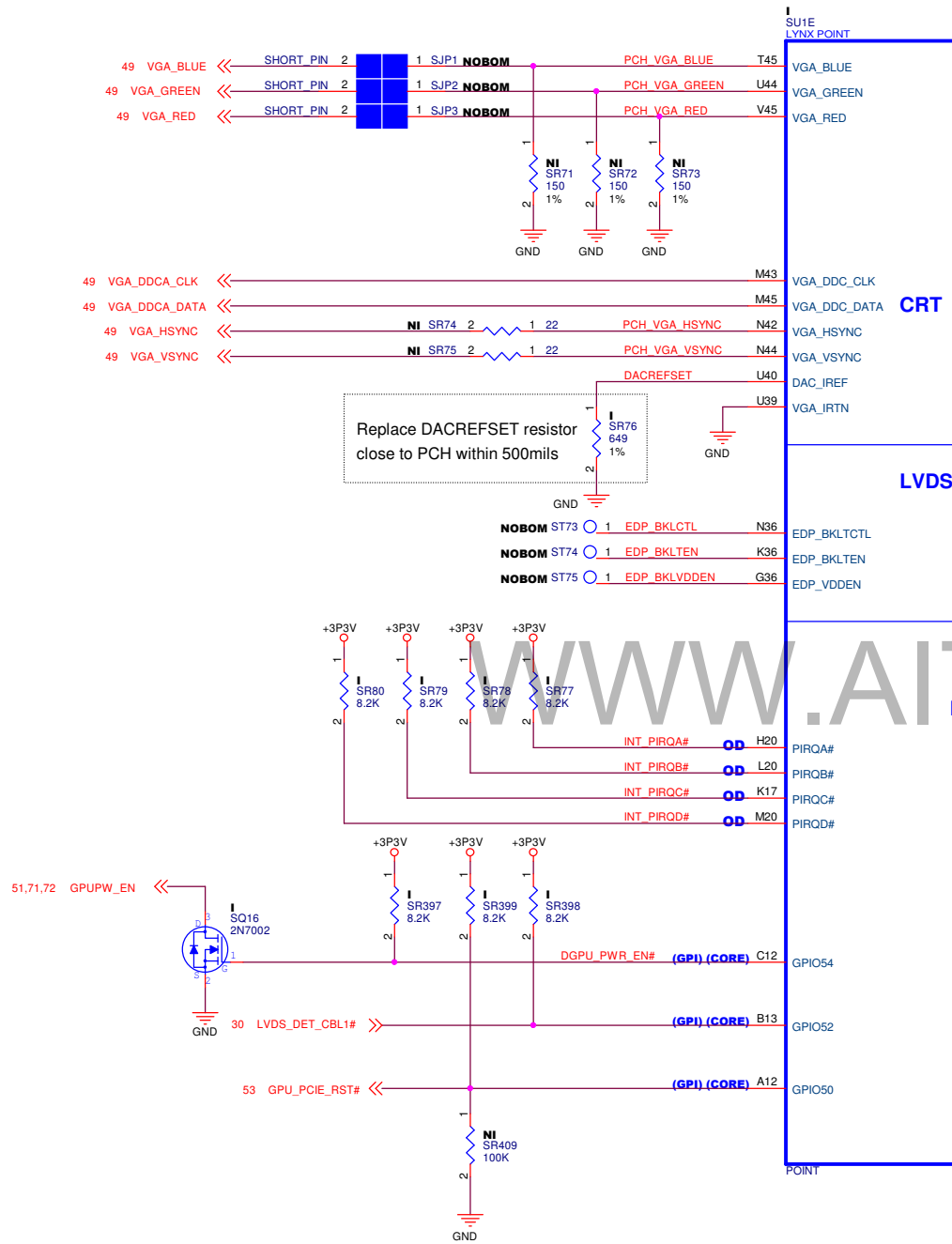


PCH CLKREQ Setting:
Not connected to device.

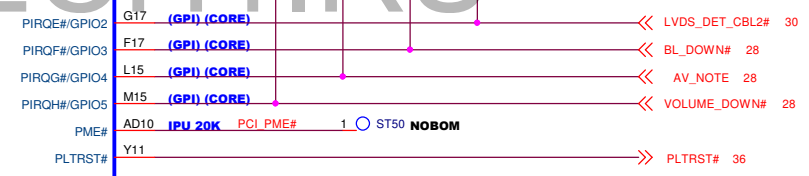
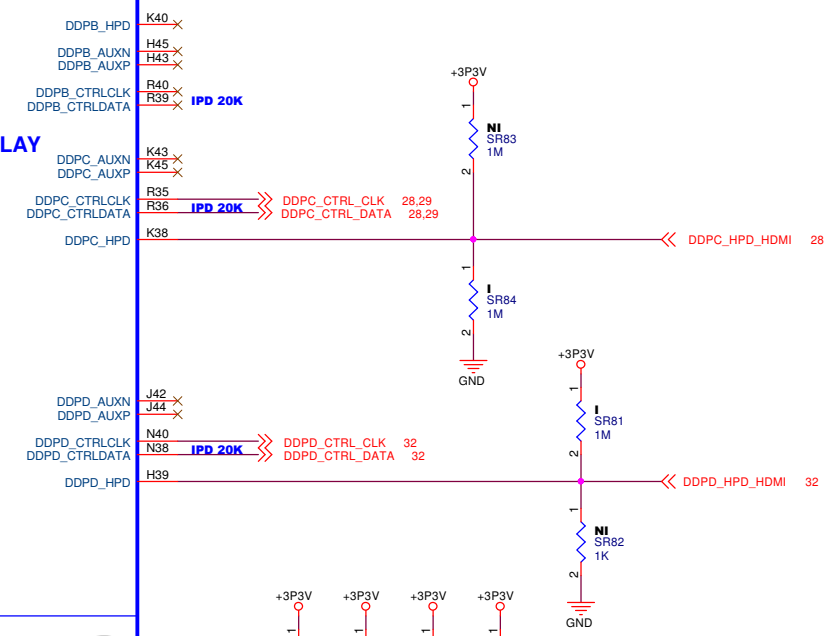


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DISPLAY



Boot select straps		
GPIO51	GPIO19	Description
0	0	LPC
1	1	SPI

GPIO49

0 : PCIe 2

1 : SATA5

CPU/Misc

GPIO

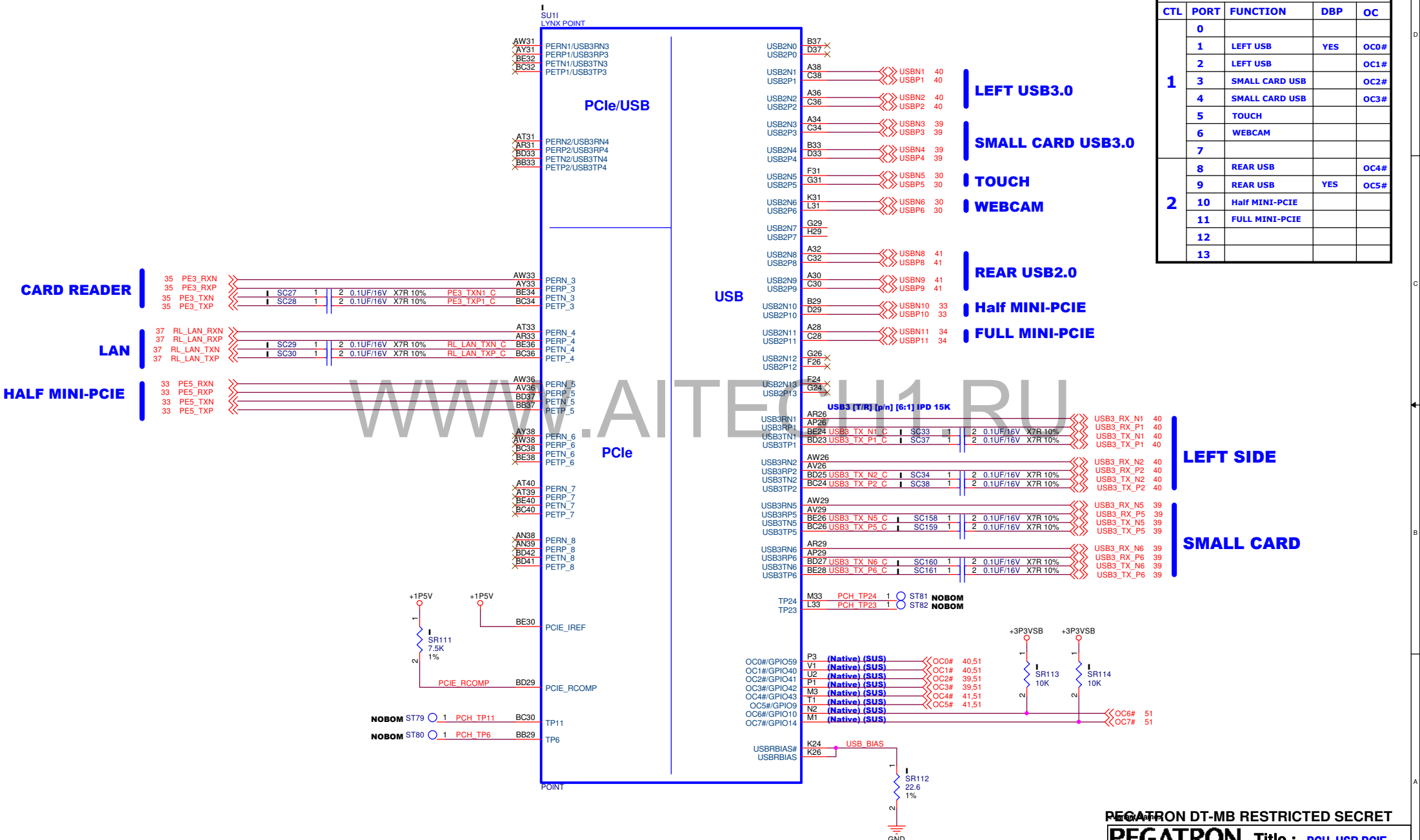
NCTF

GPIO16

0 : PCIe 1

1 : SATA4

	PCBID1	PCBID2	MBID
	GPIO1	GPIO6	GPIO22
REV1.00	0	0	GPU 0
REV1.01	1	0	UMA 1
REV1.02	0	1	
REV1.03	1	1	



USB CONTROLLER				
CTL	PORT	FUNCTION	DBP	OC
1	0			
	1	LEFT USB	YES	OC0#
	2	LEFT USB		OC1#
	3	SMALL CARD USB		OC2#
	4	SMALL CARD USB		OC3#
	5	TOUCH		
	6	WEBCAM		
2	8	REAR USB		OC4#
	9	REAR USB	YES	OC5#
	10	Half MINI-PCIE		
	11	FULL MINI-PCIE		
	12			
	13			

LEFT SIDE

SMALL CARD

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_USB,PCIE
Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00
Date: Thursday, June 27, 2013 Sheet 24 of 83		

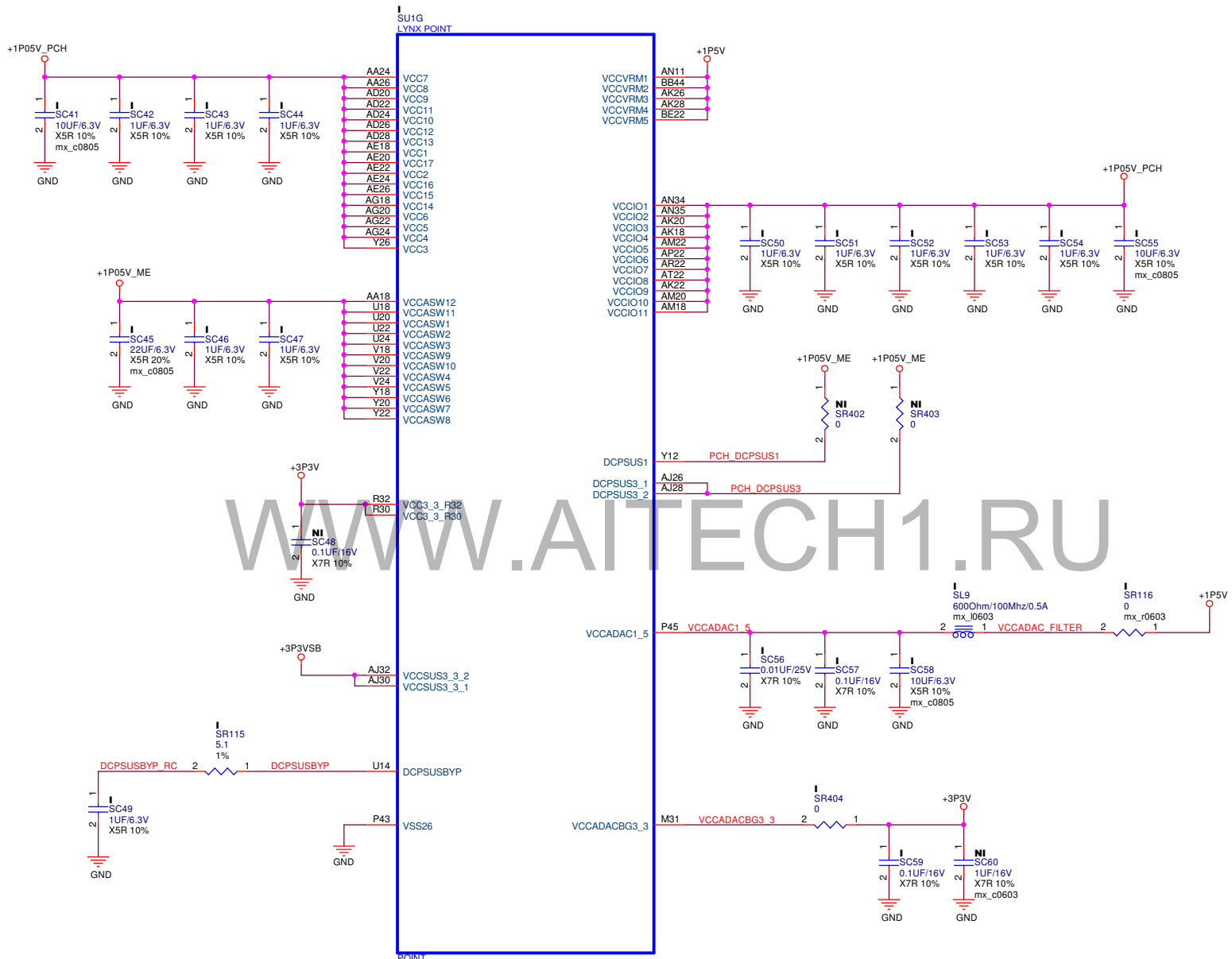
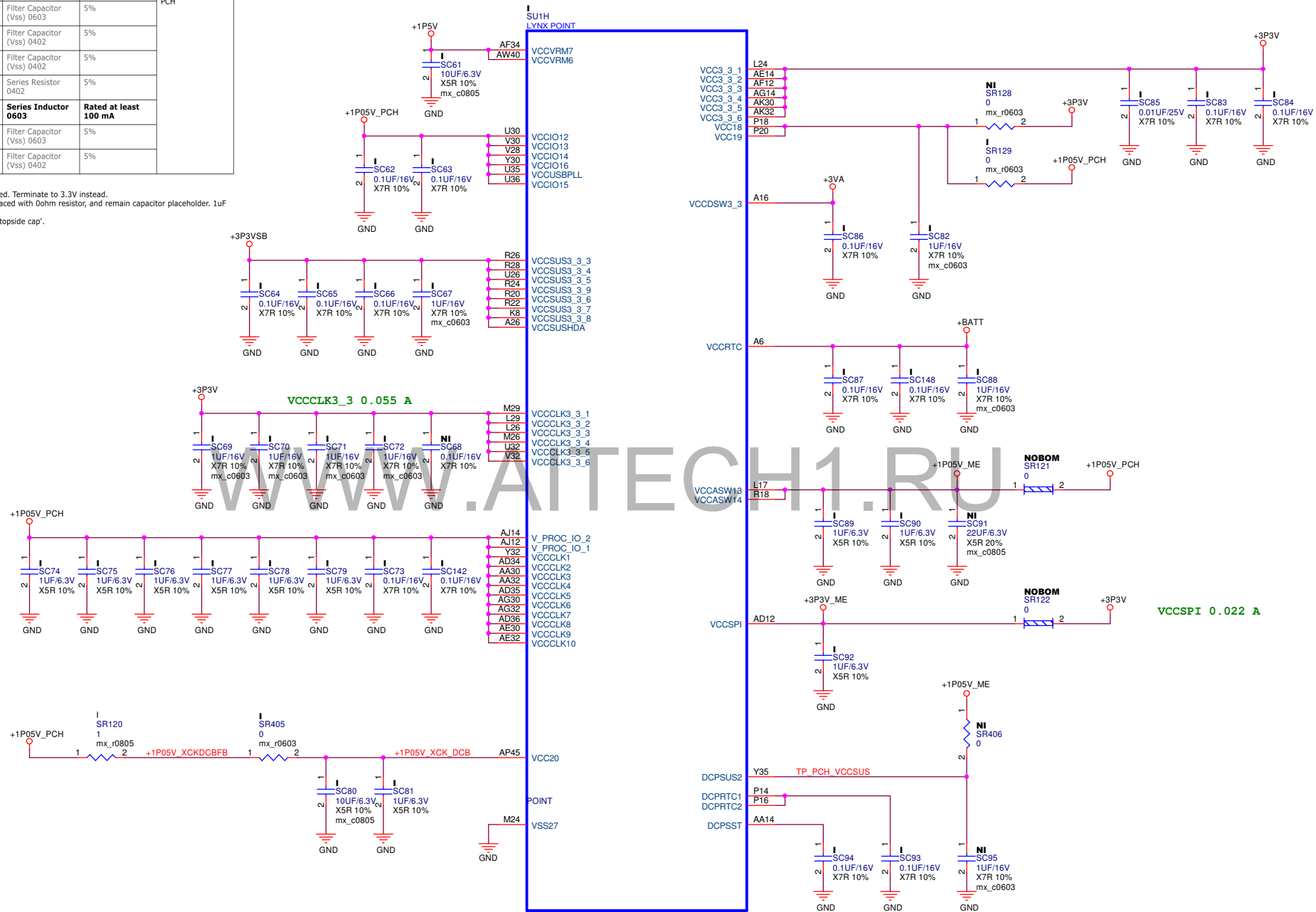


Table 35-3. Filter Requirements for PCH

Supply	Value	Quantity	Type (Pin Type)	Notes	Placement
V1.5DAC _{S0} (VccADAC Pin P45) Note 1	FB	1	Series Inductor 0603	Rated at least 100 mA	<100 mils (2.54 mm) from PCH
	10uF	1	Filter Capacitor (Vss) 0603	5%	
	0.1uF	1	Filter Capacitor (Vss) 0402	5%	
	0.01uF	1	Filter Capacitor (Vss) 0402	5%	
	1-Ohm	1	Series Resistor 0402	5%	
V1.05S (Vcc Pin AP45) Note 2	4.7uH	1	Series Inductor 0603	Rated at least 100 mA	
	10uF	1	Filter Capacitor (Vss) 0603	5%	
	1uF	1	Filter Capacitor (Vss) 0402	5%	

Notes:

1. Filter not needed if video support is disabled. Terminate to 3.3V instead.
2. For BOM cost saving, Inductor can be replaced with 0ohm resistor, and remain capacitor placeholder. 1uF BSC must be stuffed.
3. All caps are backside caps unless labeled 'topside cap'.



<Varian Name> PEGATRON DT-MB RESTRICTED SECRET

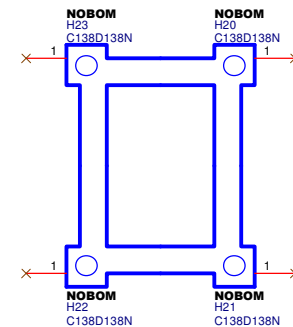
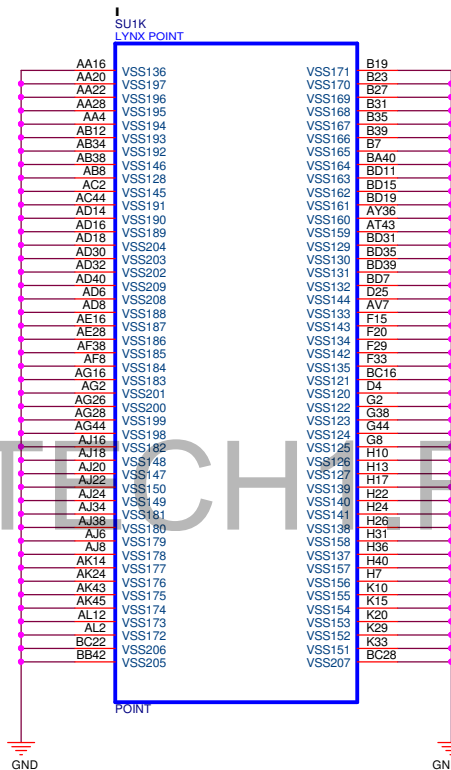
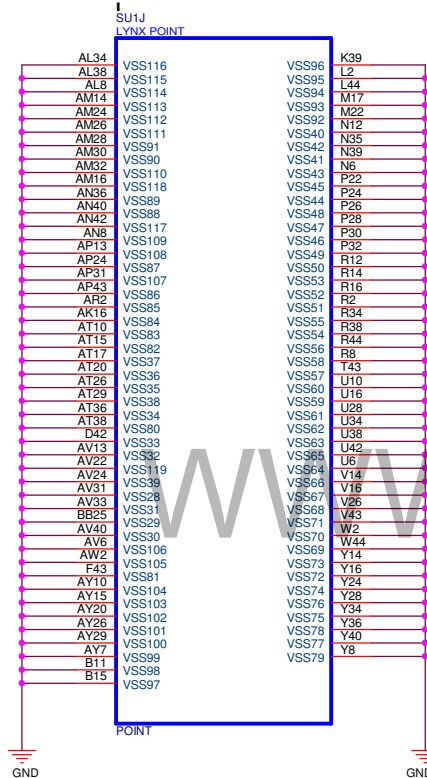
PEGATRON Title : PCH_POWER-2

Pegatron Corp. Engineer: **Stonko_Chen**

Size	Project Name	Rev
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A3	IMPLP-MS	A00
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Date: Thursday, June 27, 2013 Sheet 26 of 83



panel	PSEL0	PSEL1	PSEL2
LM215WF3(LG)	1	0	1
LM230WF3(LG)	0	0	1
HM236WU1-100(BOE)	0	1	0
M236HGJ-L21(CMI)	0	1	1
LTM230HT10(SAM)	1	0	0

From External HDMI In

31	HDMI_IN_HP				
31	SL_HDMI_B_IN_SCL				
31	SL_HDMI_B_IN_SDA				
31	SL_HDMI_B_IN_TX0P				
31	SL_HDMI_B_IN_TX1N				
31	SL_HDMI_B_IN_TX1P				
31	SL_HDMI_B_IN_TX2N				
31	SL_HDMI_B_IN_TX2P				
31	SL_HDMI_B_IN_CLKN				
31	SL_HDMI_B_IN_CLKP				

From PCH

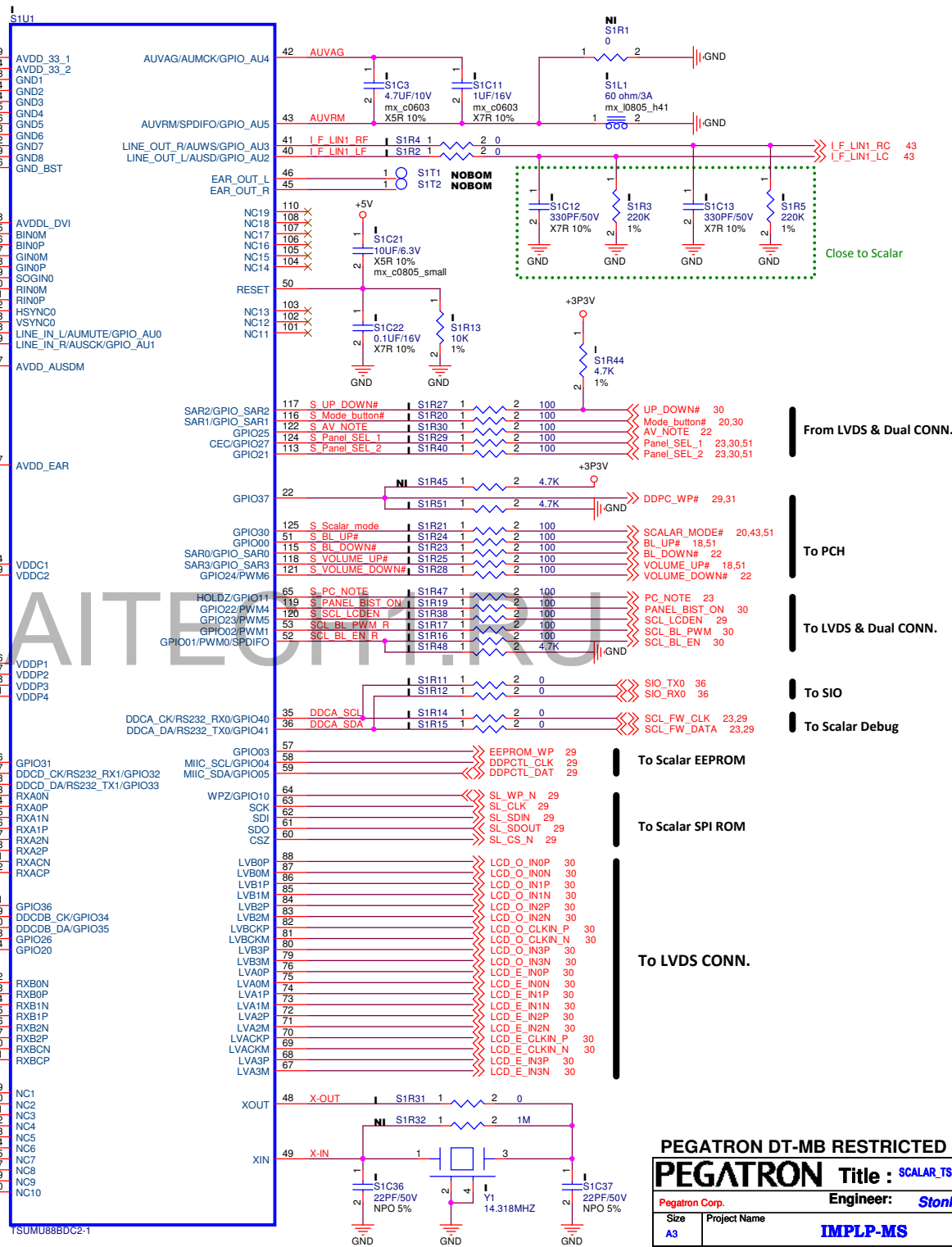
22	DDPC_HP	HDMI			
22,29	DDPC_CTRL_CLK				
22,29	DDPC_CTRL_DATA				
23	PC_Normal				
23	BIST_ON				

From Internal CPU HDMI In

8	HDMIC_TMDSC_DATA0#				
8	HDMIC_TMDSC_DATA0				
8	HDMIC_TMDSC_DATA1#				
8	HDMIC_TMDSC_DATA1				
8	HDMIC_TMDSC_DATA2#				
8	HDMIC_TMDSC_DATA2				
8	HDMIC_TMDSC_CLK#				
8	HDMIC_TMDSC_CLK				

To LEVEL SHIFT

29	HDMI_LS_CLK				
29	HDMI_LS_CLK#				
29	HDMI_LS_D2				
29	HDMI_LS_D2#				
29	HDMI_LS_D1				
29	HDMI_LS_D1#				
29	HDMI_LS_D0				
29	HDMI_LS_D0#				



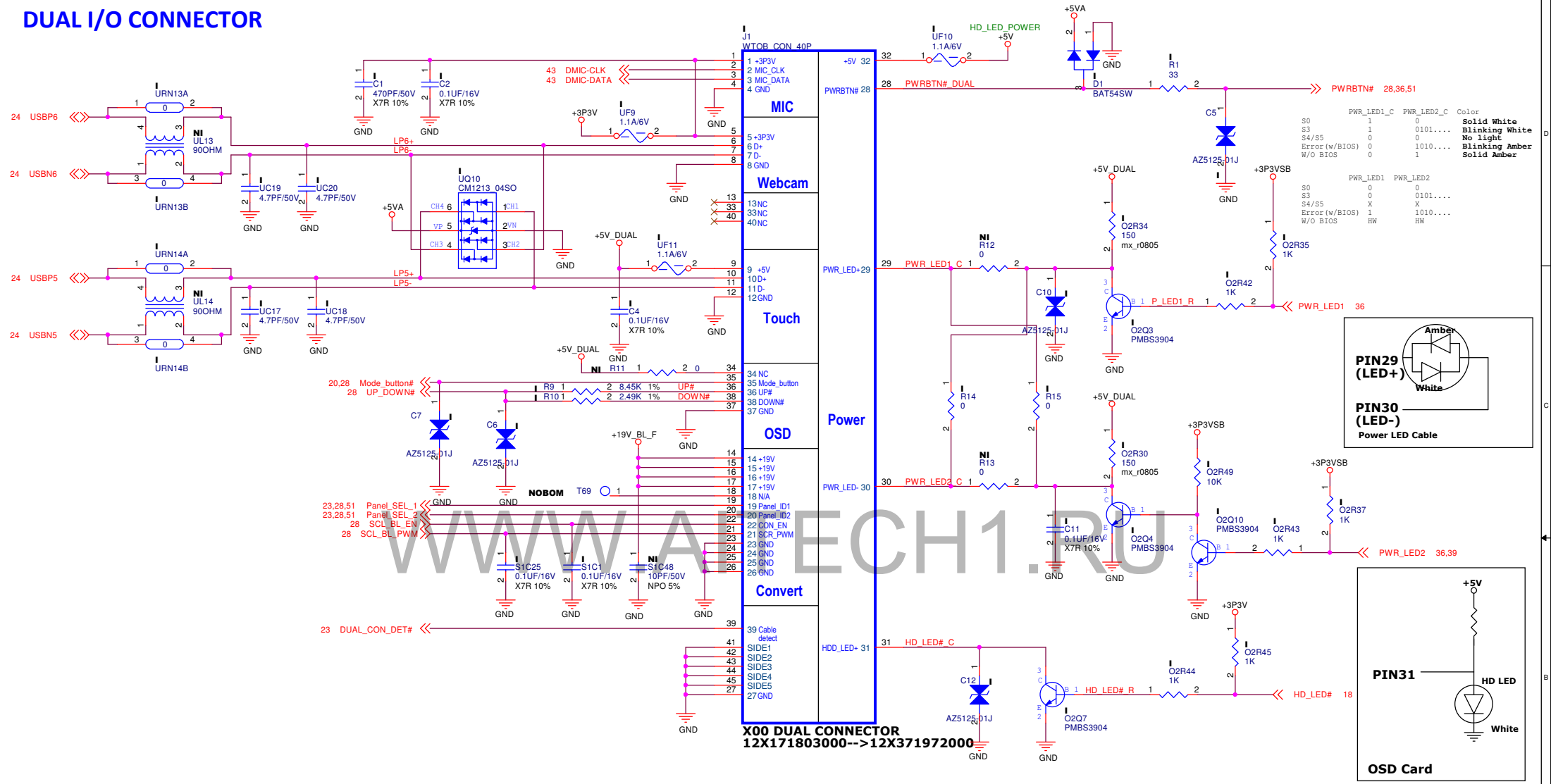
PEGATRON Title : SCALAR_TSUMU88BDC2-1

Size	Project Name	Rev
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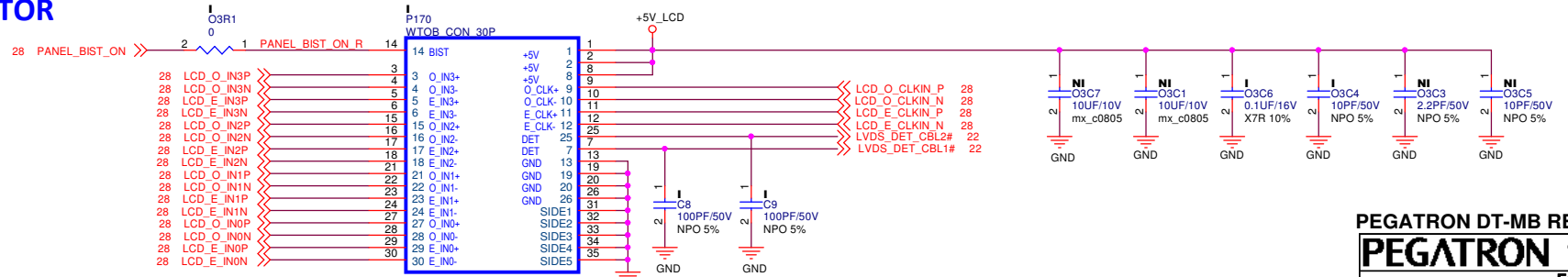
A3	IMPLP-MS	A00
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Date: Thursday, June 27, 2013 Sheet 28 of 83

DUAL I/O CONNECTOR



LVDS CONNECTOR



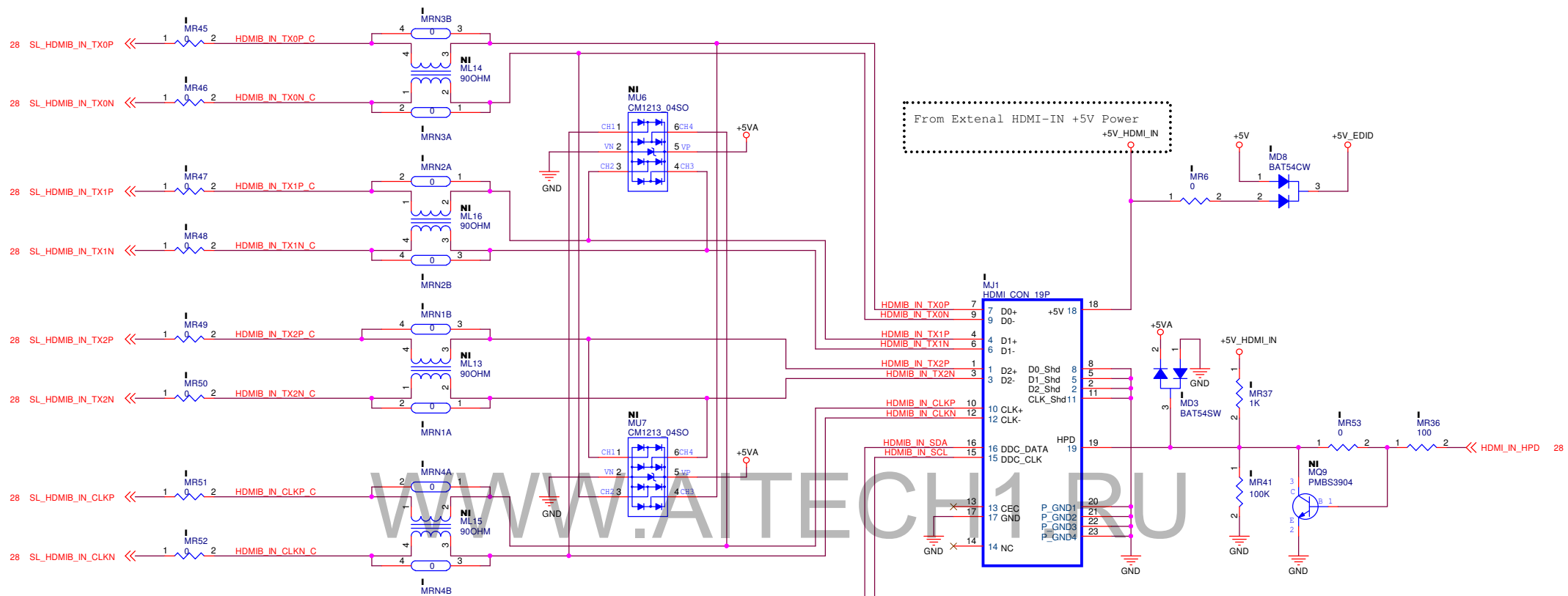
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CABLE CONNECTOR

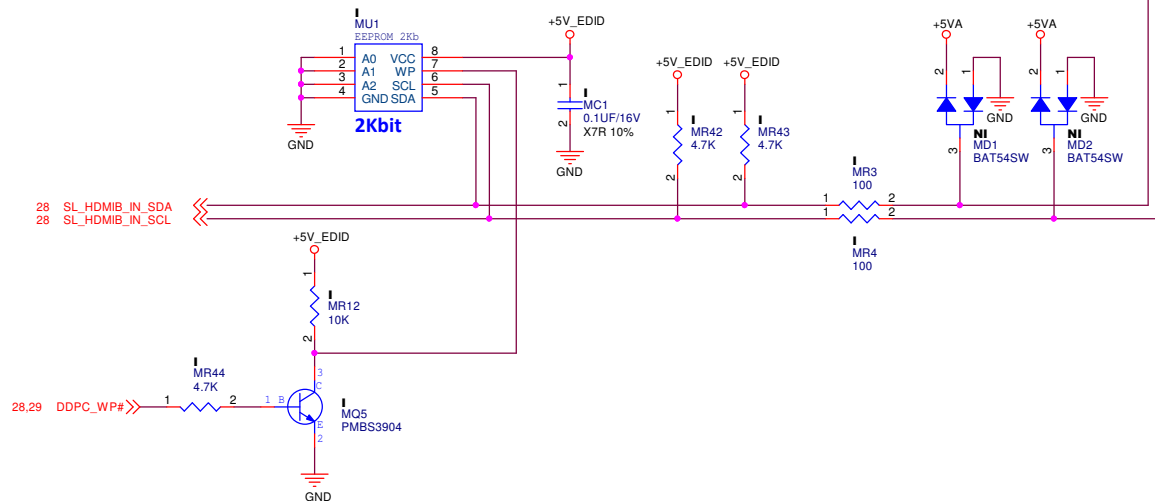
Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name IMPLP-MS Rev A00

Date: Thursday, June 27, 2013 Sheet 30 of 83



EXTERNAL HDMI IN EDID



PEGATRON DT-MB RESTRICTED SECRET

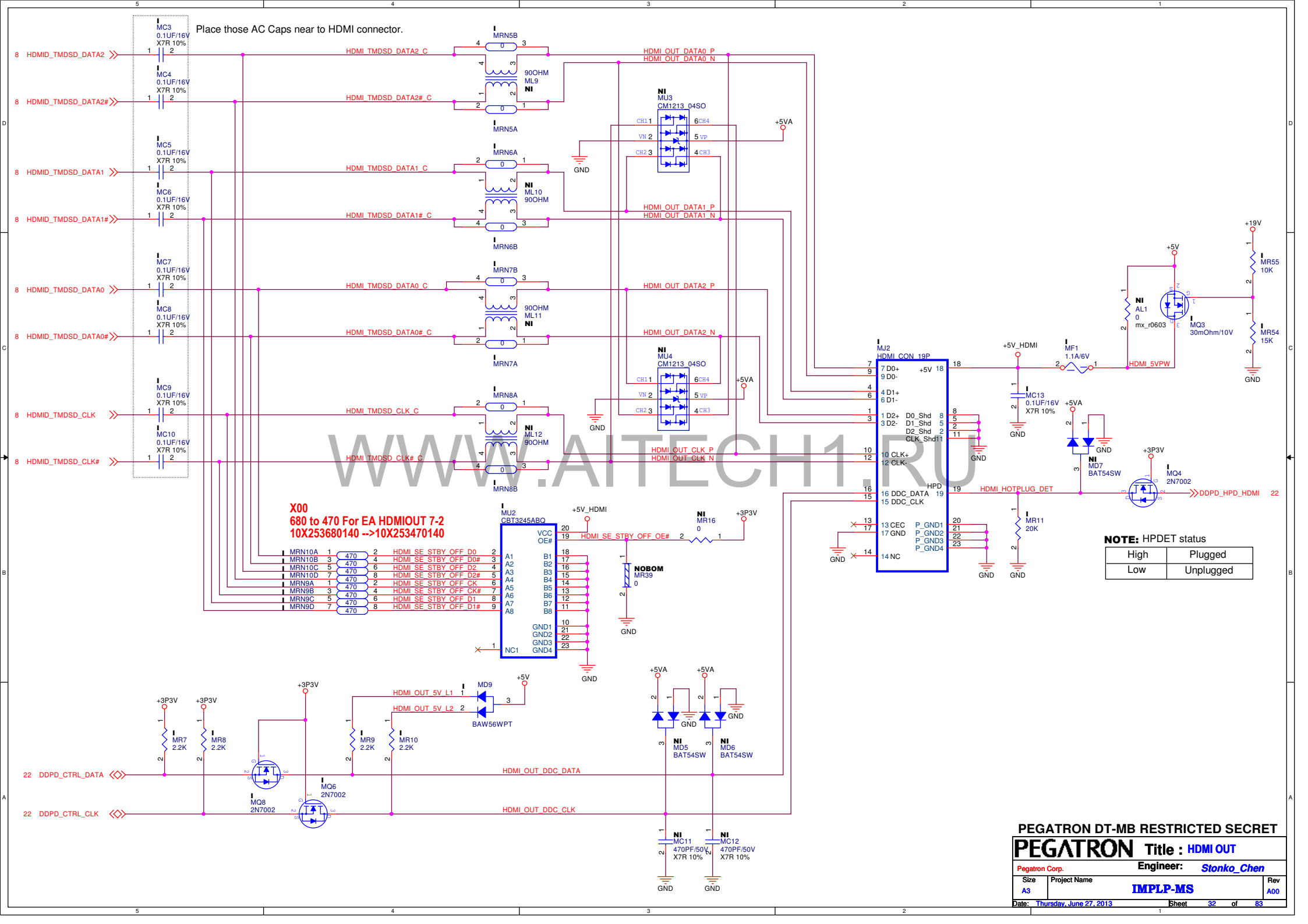
PEGATRON Title : **HDMI_IN**

Pegatron Corp. Engineer: **Stonko_Chen**

Size A3 Project Name **IMPLP-MS** Rev A00

Date: Thursday, June 27, 2013 Sheet 31 of 83

Place those AC Caps near to HDMI connector.



PEGATRON DT-MB RESTRICTED SECRET

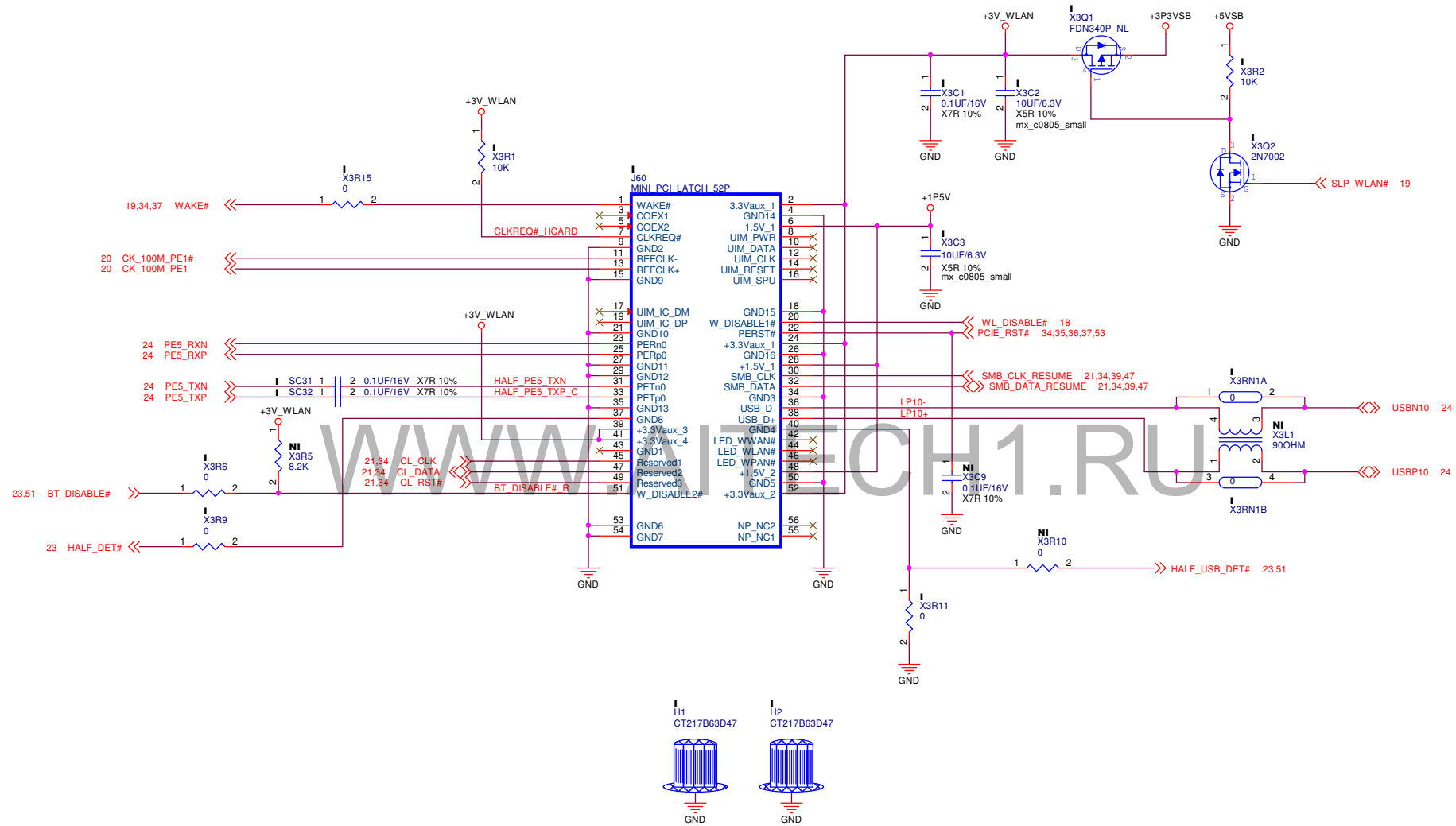
PEGATRON Title : HDMI OUT

Pegatron Corp. Engineer: **Stonko_Chen**

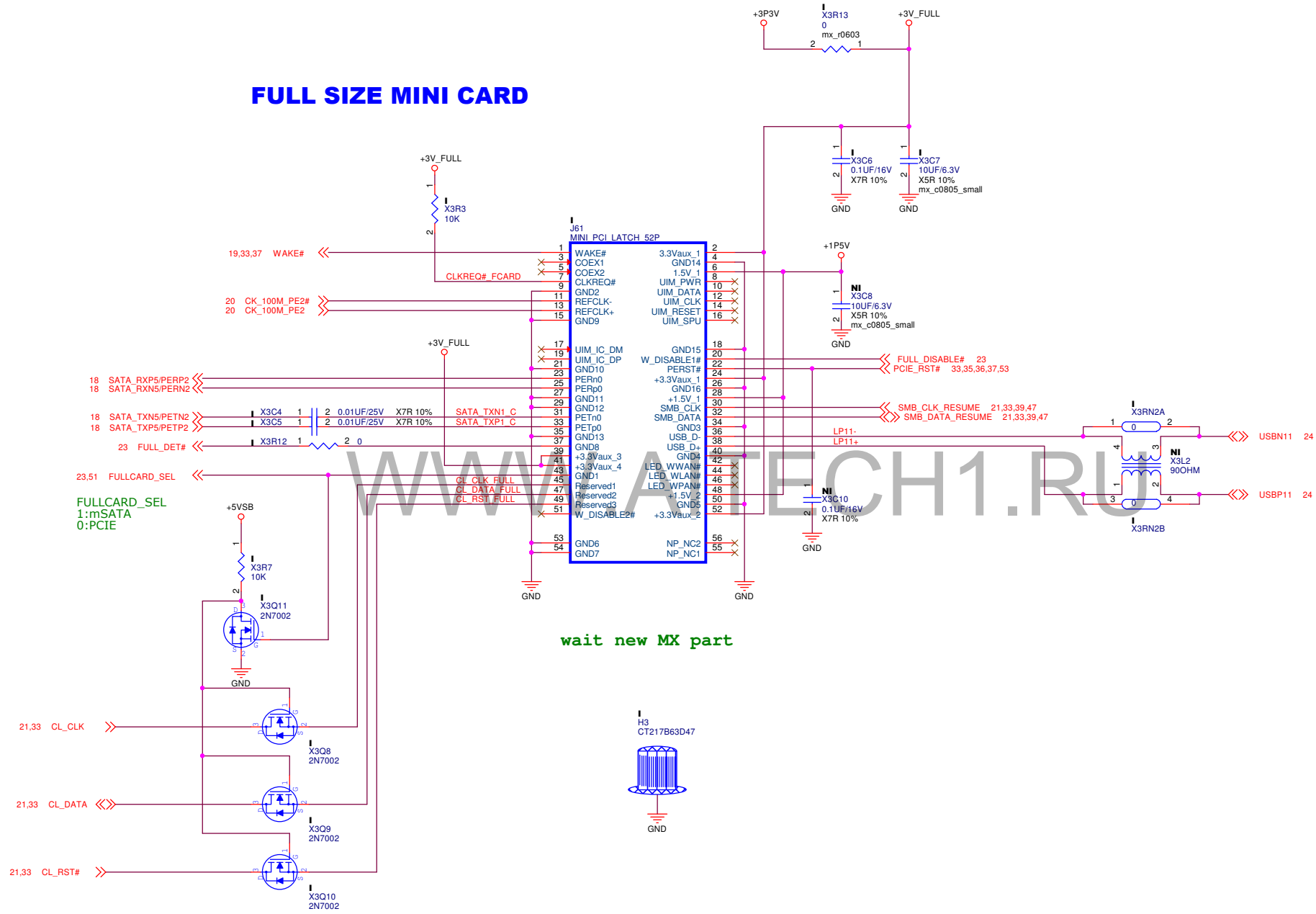
Size A3	Project Name IMPLP-MS	Rev A00
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HALF SIZE MINI CARD



FULL SIZE MINI CARD



wait new MX part

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FULL MINI-PCIE

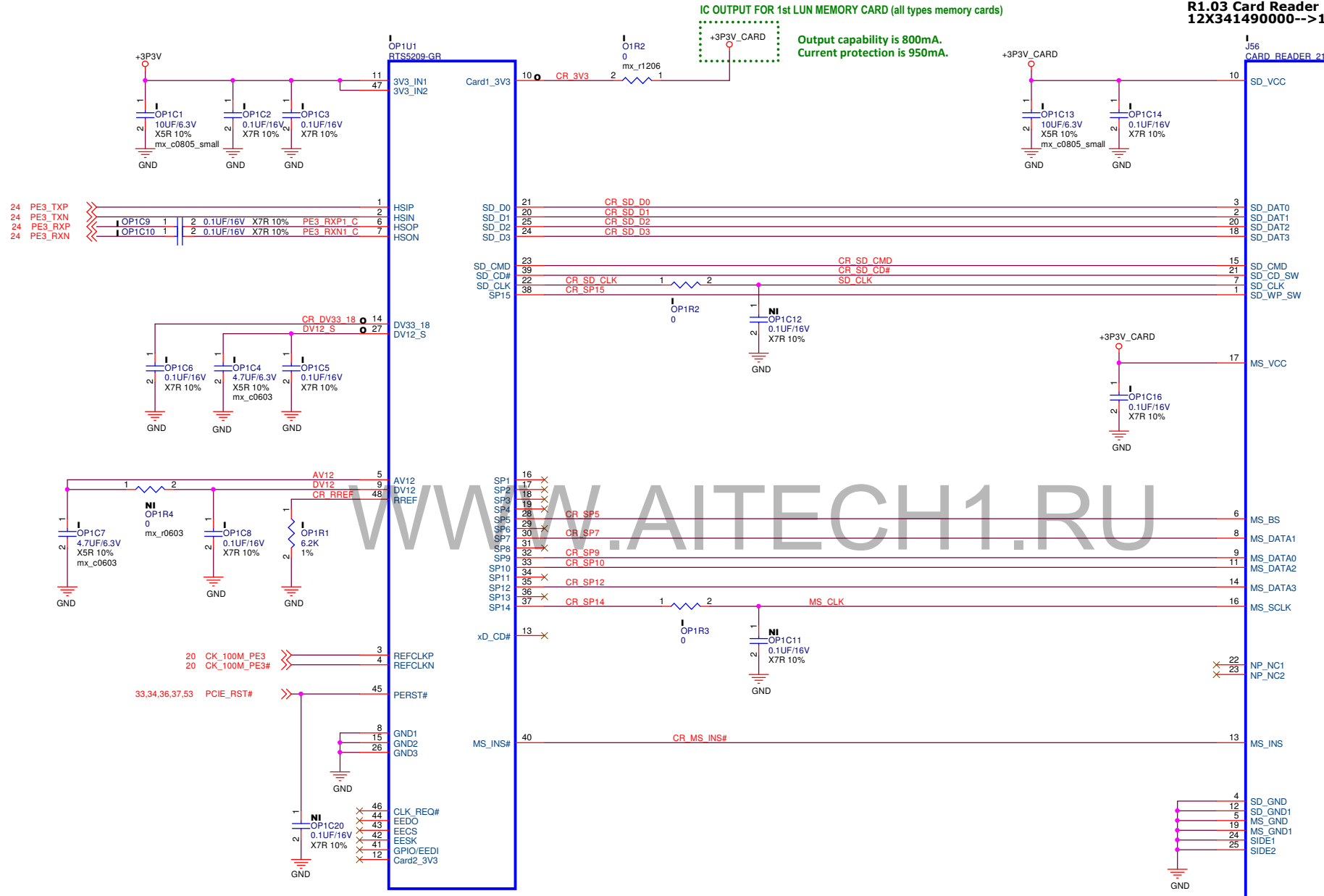
Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name IMPLP-MS Rev A00

Date: Thursday, June 27, 2013 Sheet 34 of 83

CARDREADER RST5209

X00 Card Reader
12XC4CE42001-->12X341490000
R1.03 Card Reader
12X341490000-->12XC3C321000



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CARDREADER RST5209
Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00
Date: Thursday, June 27, 2013	Sheet 35 of 83	

Pin 14/15/16/17:
1. Please check if this pin need be pull-up on chipset side!
2. If you do not use the KBC, please pull-up these pin to +5VSB.

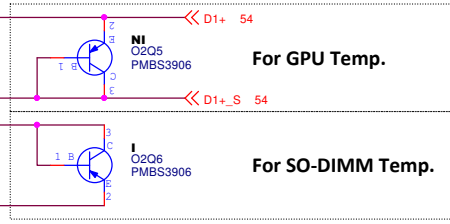
Pin 3: SERIRQ
Please check if this pin need be pull-up on chipset side!

PIN15	ME
H	EN
L	Disable

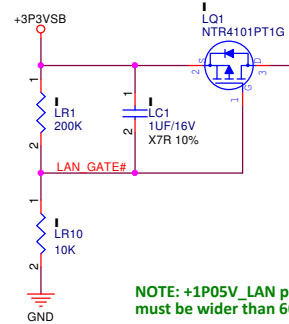
1: PWOK (pin 35) for AMD (Default)
0: PWOK (pin 35) for Intel

If you do not use the UART port, Pin 53/55/58/60: please pull-up these pin to +3P3V
Pin 54: please pull-up these pin to +3P3VSB

Pin 27:
SIO invert internally SLP_SUS from PCH and output ERP_CTRL0# to control DSW.
Pin 59:
1: Configuration Register I/O port is 4E/4F.(Default)
0: Configuration Register I/O port is 2E/2F.

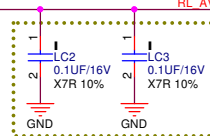


NOTE: +3P3VSB power trace must be wider than 40 mils

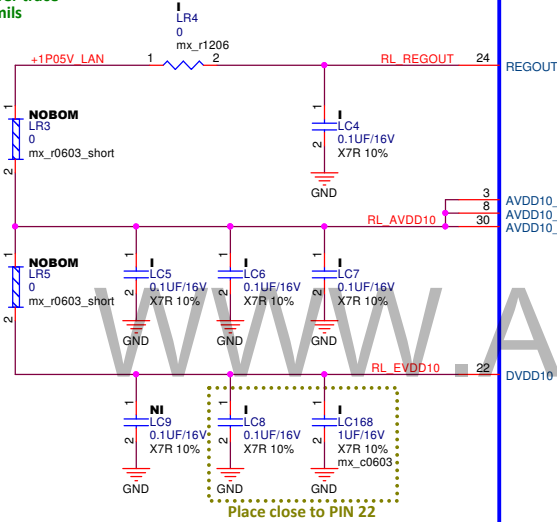


NOTE: +1P05V_LAN power trace must be wider than 60 mils

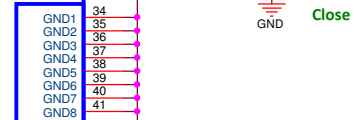
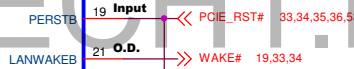
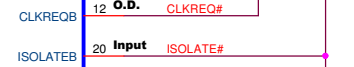
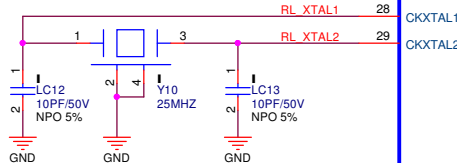
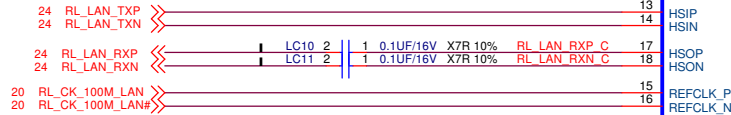
For RTL8151G(S)D
* Place C1 and C2 close to each VDD33 pin-- 11, 32



RTL8151GSD: Switching Regulator 1.0V Output
RTL8151GD: LDO Regulator 1.0V Output



For RTL8151G(S)D
* Place LC4 to LC8 close to each VDD10 pin-- 3, 8, 22, 30



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor LR8 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5. If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

ISOLATEB	I	20	Isolate Pin: Active low. Used to isolate the RTL8151GD/RTL8151GSD from the PCI Express bus. The RTL8151GD/RTL8151GSD will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.
----------	---	----	---

LANWAKEB	O/D	21	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
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Please make sure WAKE# has been pulled up +3P3VSB through 10K on PCH side (Realtek recommendation).

Close to LAN chip

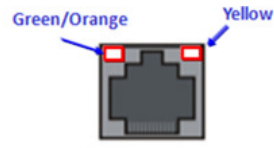
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LAN RTL8151GD

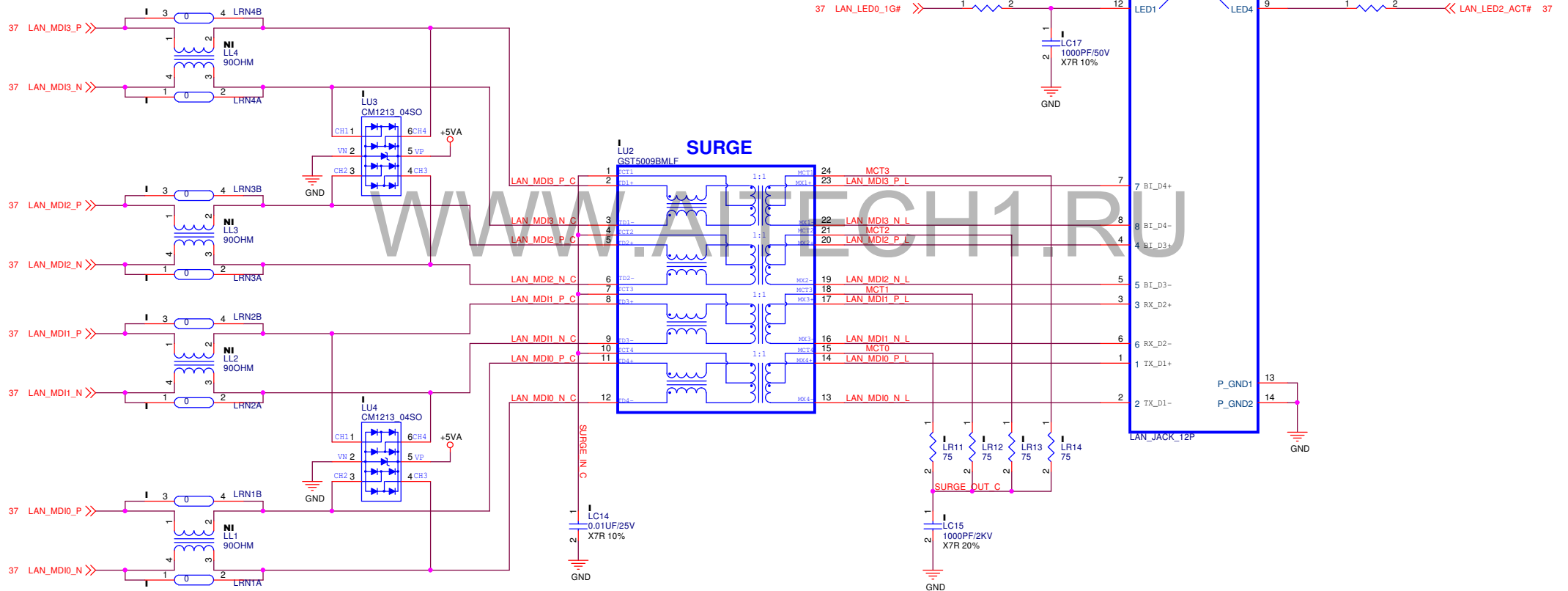
Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name IMPLP-MS

Date: Thursday, June 27, 2013 Sheet 37 of 83



Function	LINK LED State/Color	Active LED State/Color
No Link	OFF/ NA	OFF/ NA
Link 10Mbps	ON/Green	
Link 100Mbps	ON/Green	
Link 1000Mbps	ON/Orange	
No network activity		OFF/ NA
Network activity		Blinking/Yellow



PEGATRON DT-MB RESTRICTED SECRET

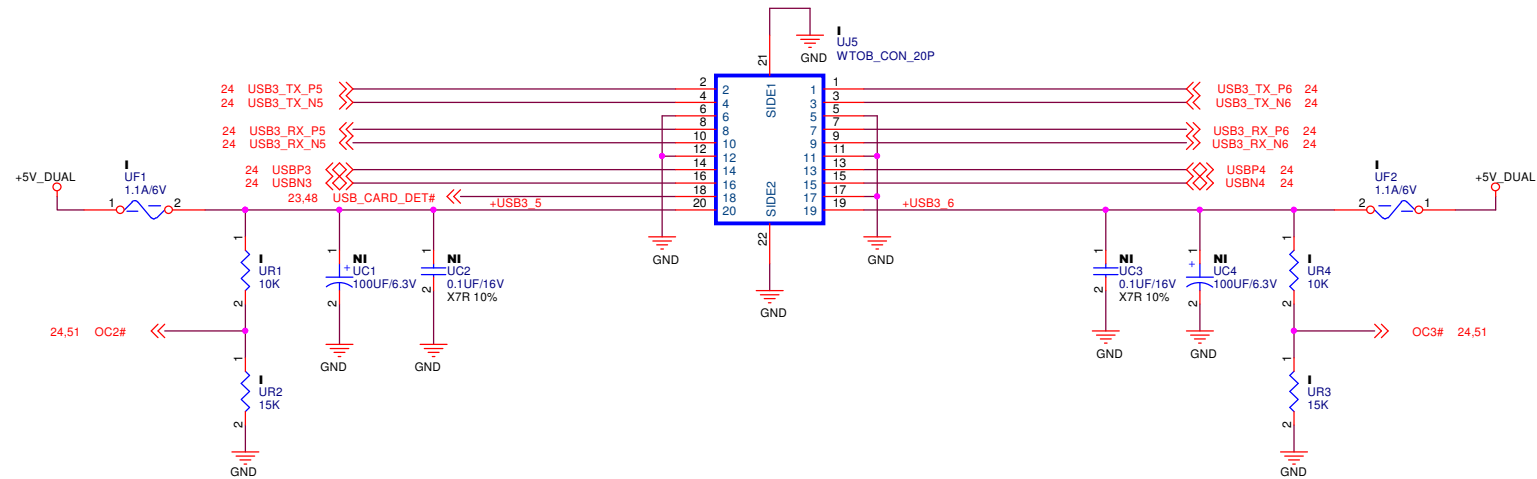
PEGATRON Title : **RJ45 CONN.**

Pegatron Corp. Engineer: **Stonko_Chen**

Size A3	Project Name IMPLP-MS	Rev A00
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Date: Thursday, June 27, 2013 Sheet 38 of 83

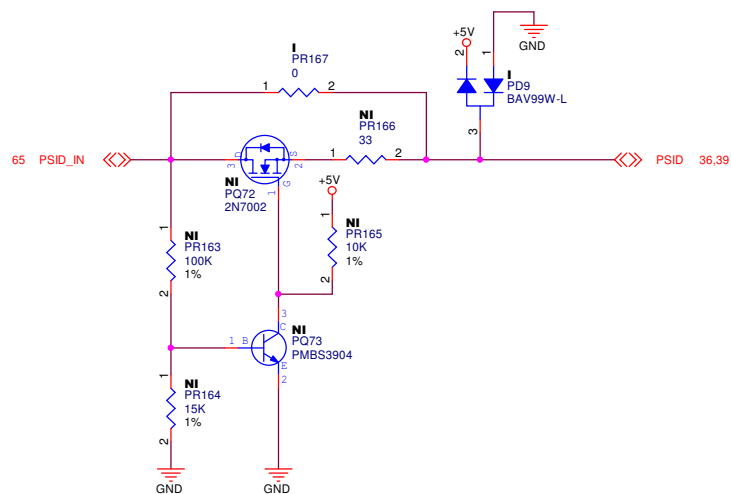
TO USB CARD CONNECTOR



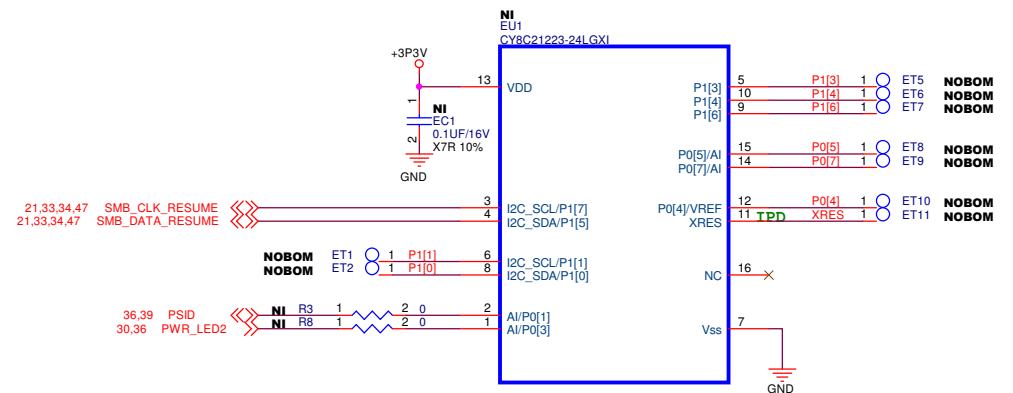
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PSID CIRCUIT

IF don't use PSID circuit Integrated PR167, NI Other
IF use PSID circuit NI PR167



EC FOR ADAPTER PSID



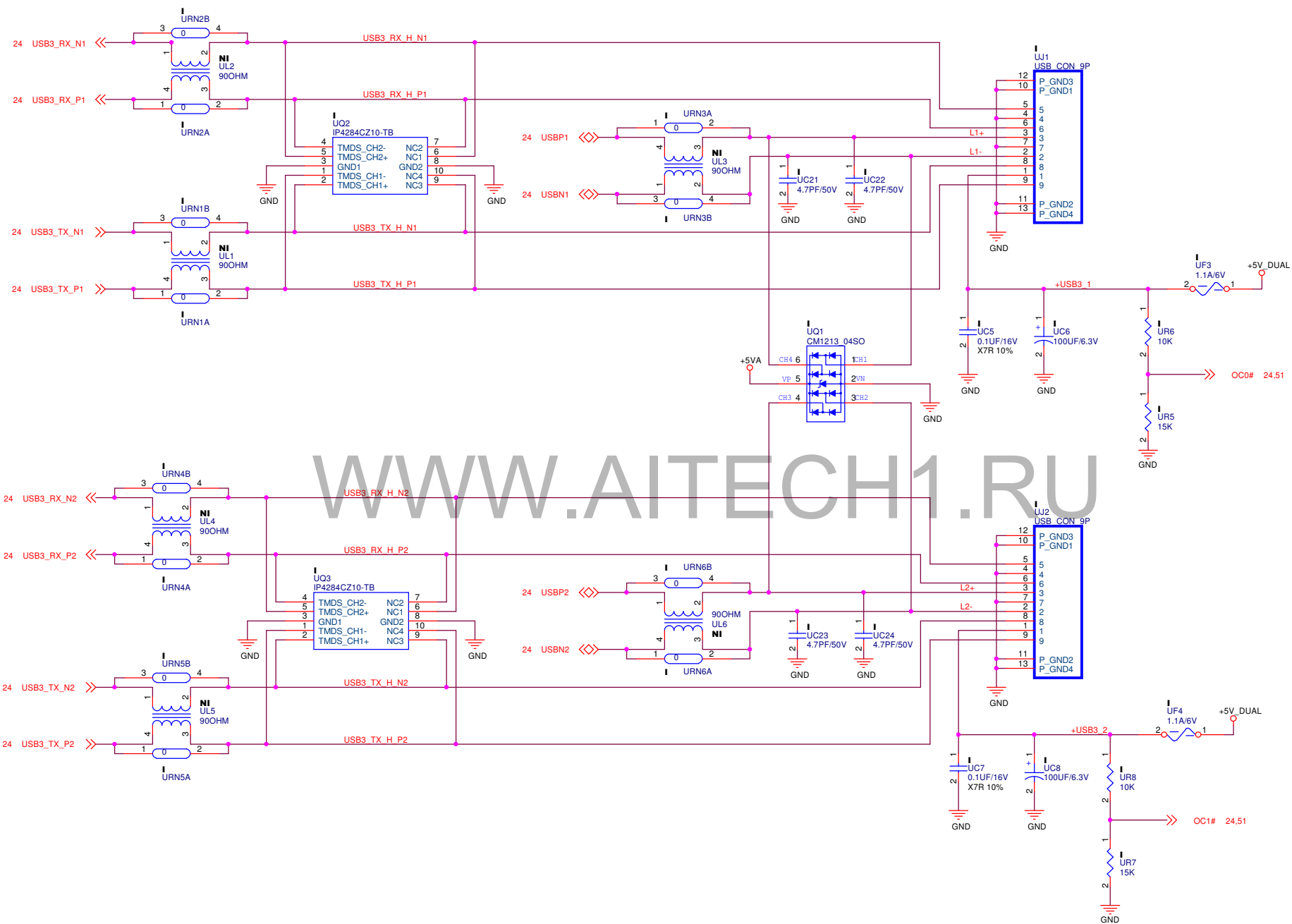
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB&AUDIO CARD&EC

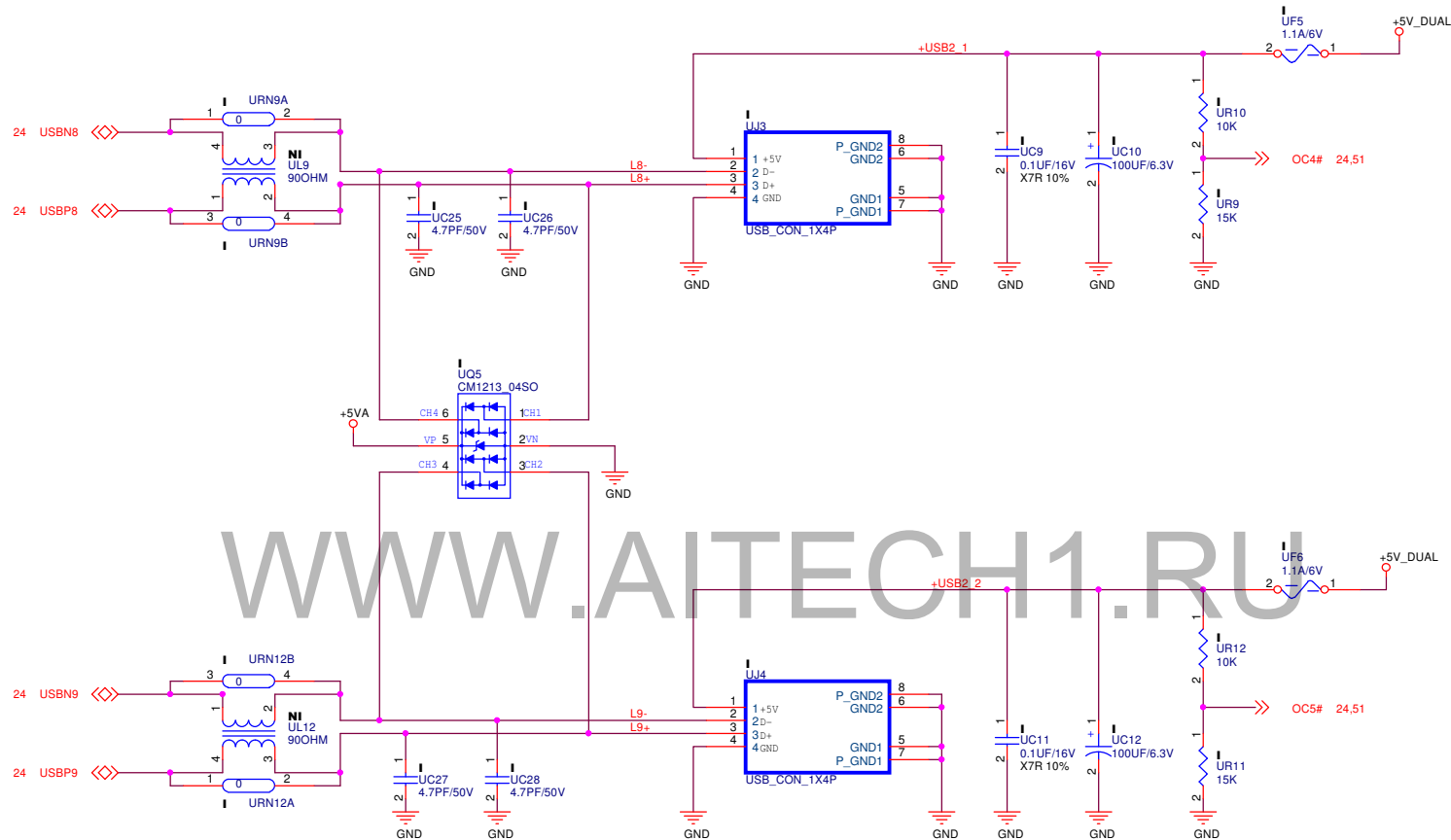
Pegatron Corp. Engineer: **Stonko_Chen**

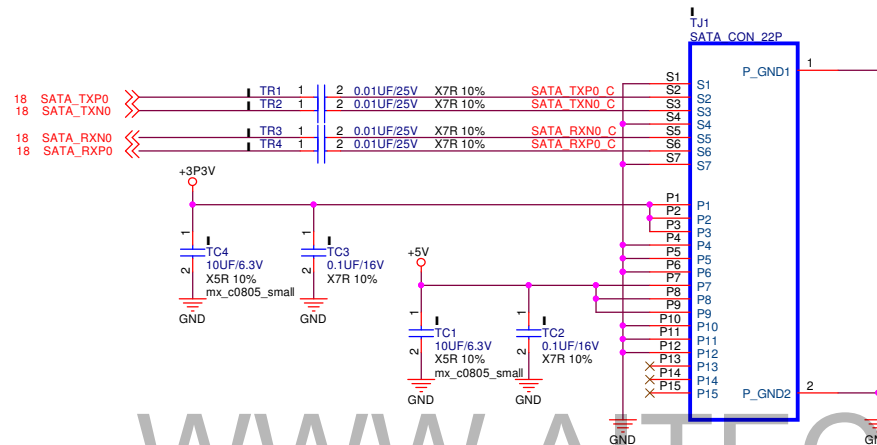
Size	Project Name	Rev
A3	IMPLP-MS	A00

Date: Thursday, June 27, 2013 Sheet 39 of 83



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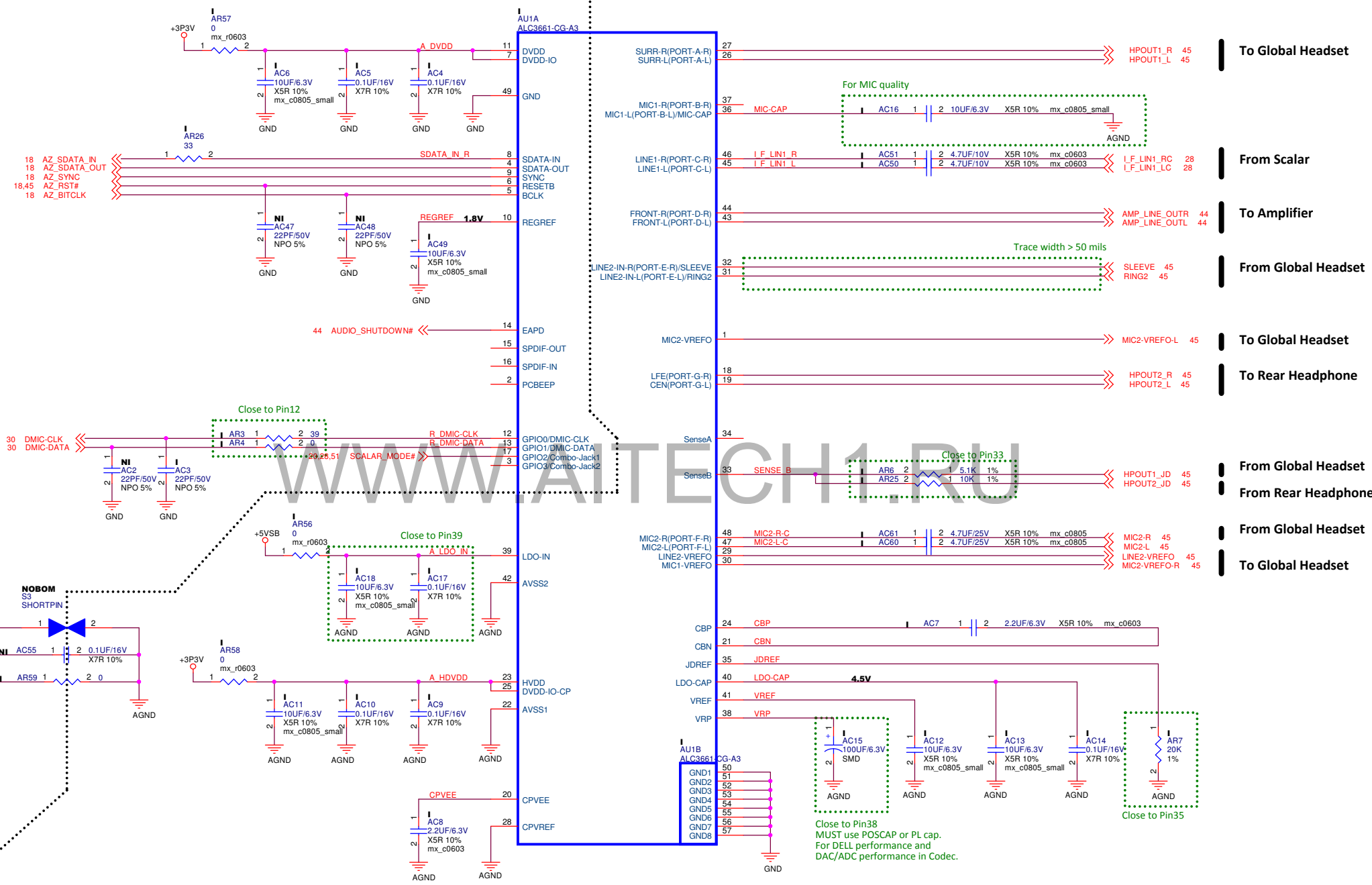




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GHS JACK
12X241667000 -->12X241998000

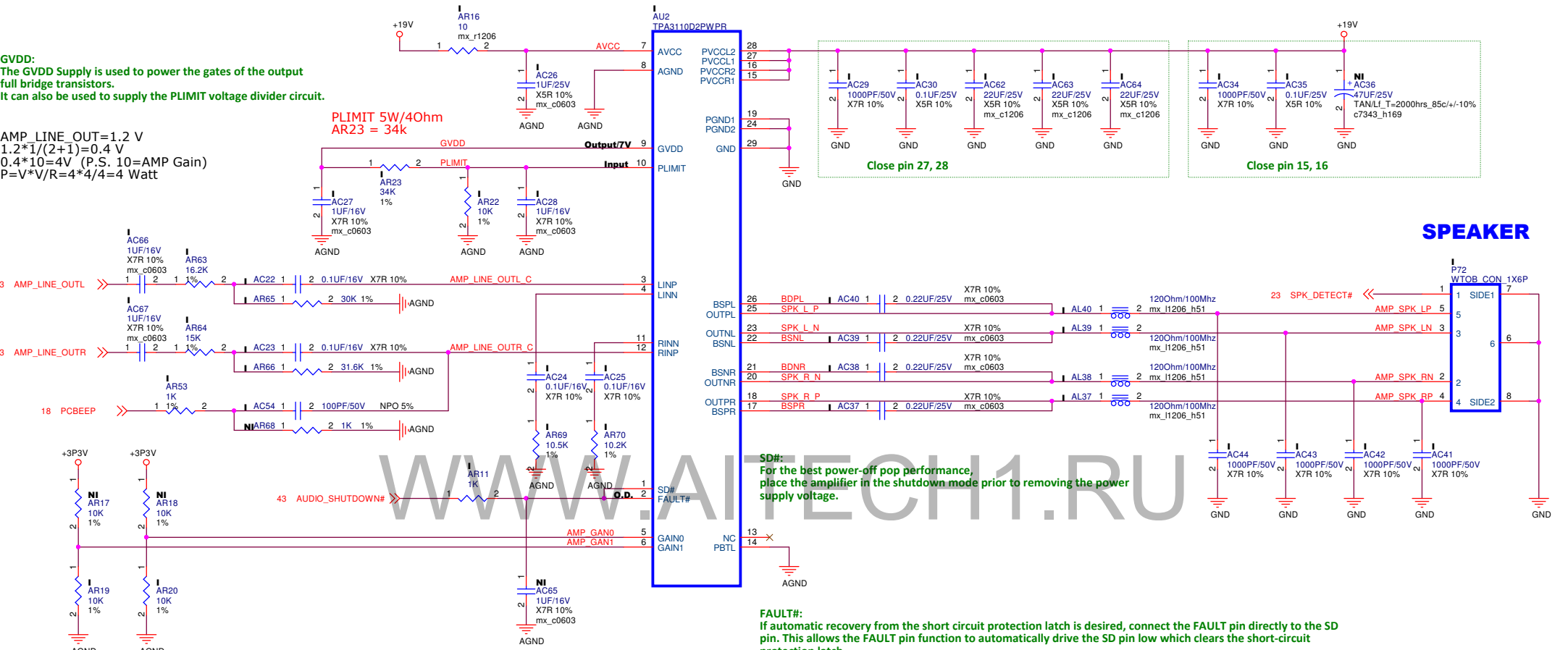
ALC3661 CODEC



AUDIO AMPLIFIER

GVDD:
The GVDD Supply is used to power the gates of the output full bridge transistors.
It can also be used to supply the PLIMIT voltage divider circuit.

AMP_LINE_OUT=1.2 V
1.2*1/(2+1)=0.4 V
0.4*10=4V (P.S. 10=AMP Gain)
P=V*V/R=4*4/4=4 Watt



GAIN1	GAIN0	AMP GAIN (dB)	INPUT IMPEDANCE (k Ohm)
0	0	20dB (10)	60
0	1	26dB (20)	30
1	0	32dB (40)	15
1	1	36dB (80)	9

PLIMIT:
The PLIMIT circuit sets a limit on the output peak-to-peak voltage.
This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S} \right) \times V_p \right)^2}{2 \times R_L}$$
 for unclipped power

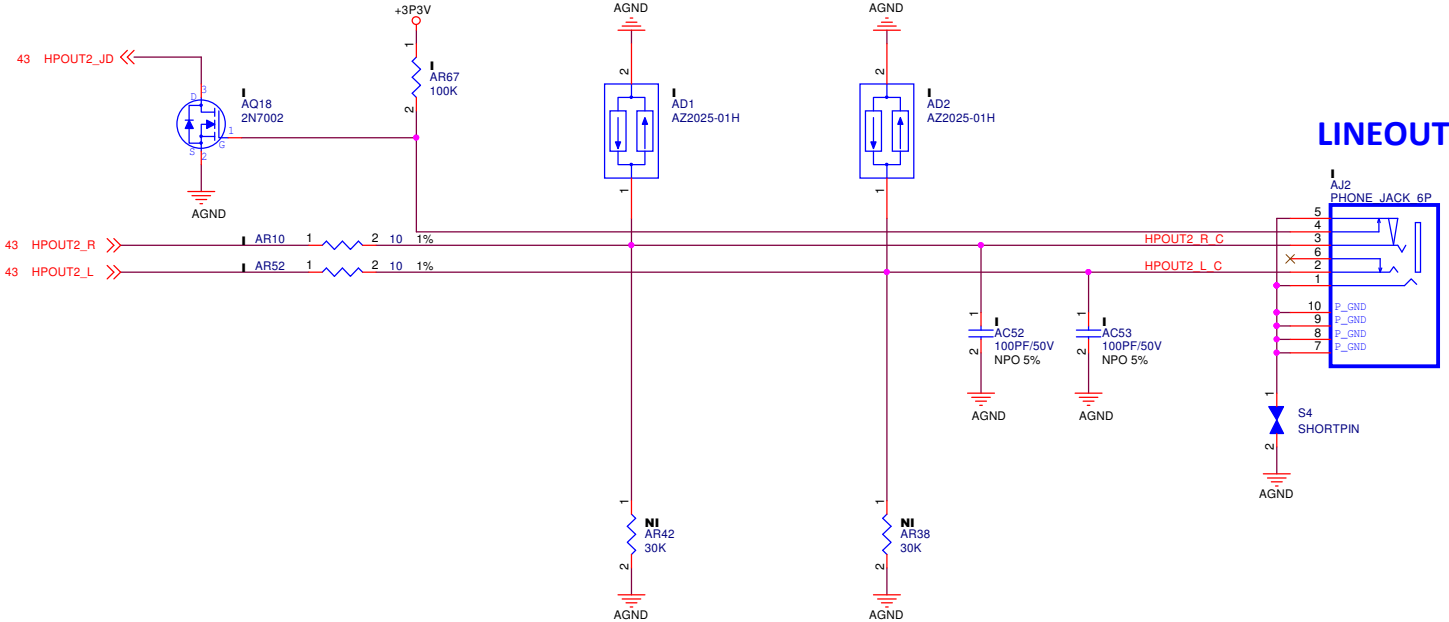
Where:
R_S is the total series resistance including R_{DS(on)}, and any resistance in the output filter.
R_L is the load resistance.
V_P is the peak amplitude of the output possible within the supply rail.
V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

SD#:
For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

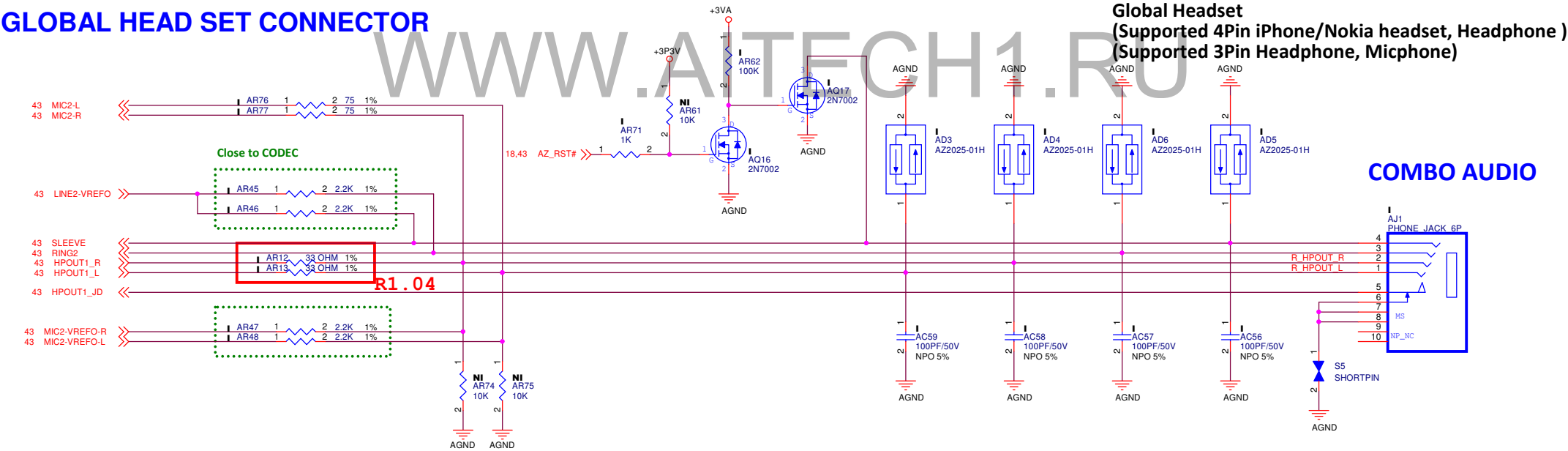
FAULT#:
If automatic recovery from the short circuit protection latch is desired, connect the FAULT pin directly to the SD pin. This allows the FAULT pin function to automatically drive the SD pin low which clears the short-circuit protection latch.

PBTL:
H→the positive and negative outputs of each channel (left and right) are synchronized and in phase.
L→For normal BTL operation, connect the PBTL pin to local ground.

REAR LINE-OUT
No Support Re-Tasking Function



GLOBAL HEAD SET CONNECTOR



GHS JACK
12X141608000 --> 12X141940000

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : REAR HP-OUT & GHS CONN.

Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name IMPLP-MS Rev A00

Date: Thursday, June 27, 2013 Sheet 45 of 83

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<Pegatron DT-MB RESTRICTED SECRET

PEGATRON

Title : AUDIO MUTE

Pegatron Corp.

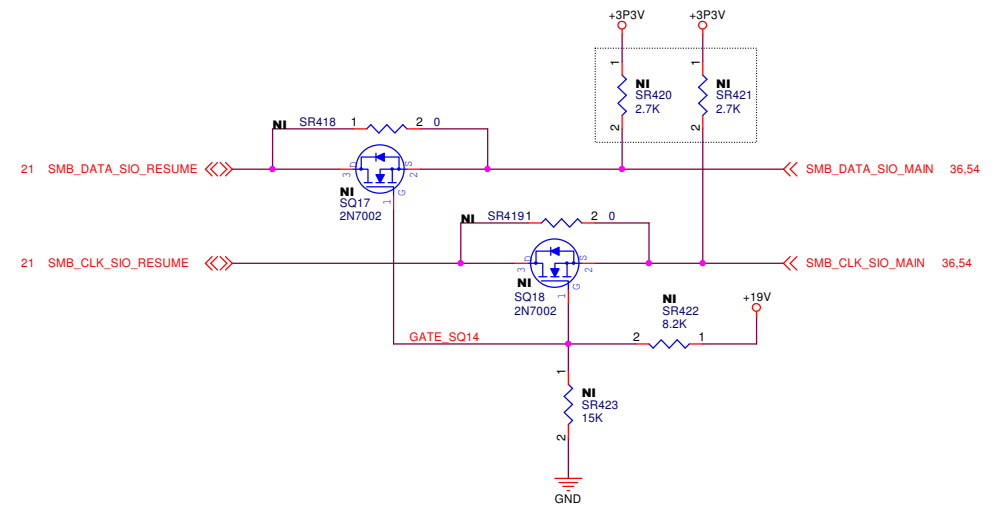
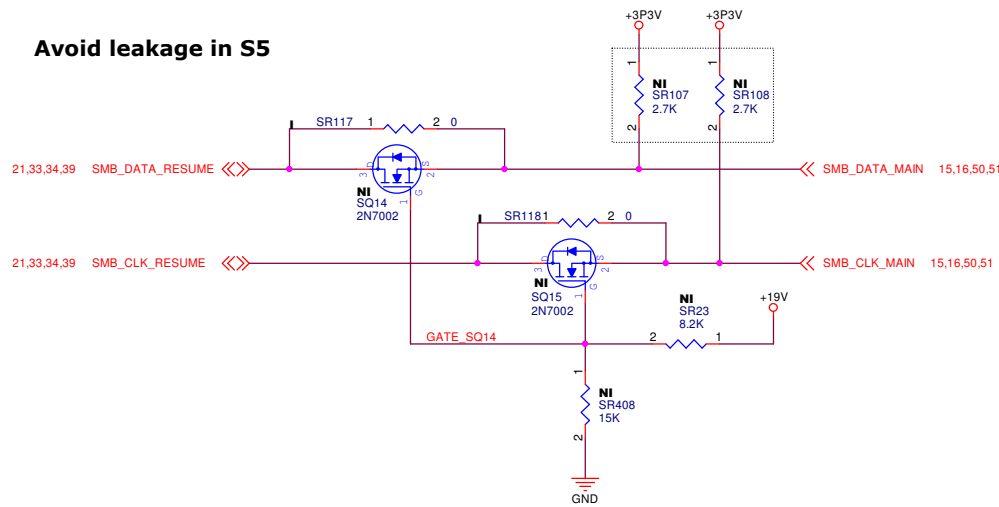
Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00

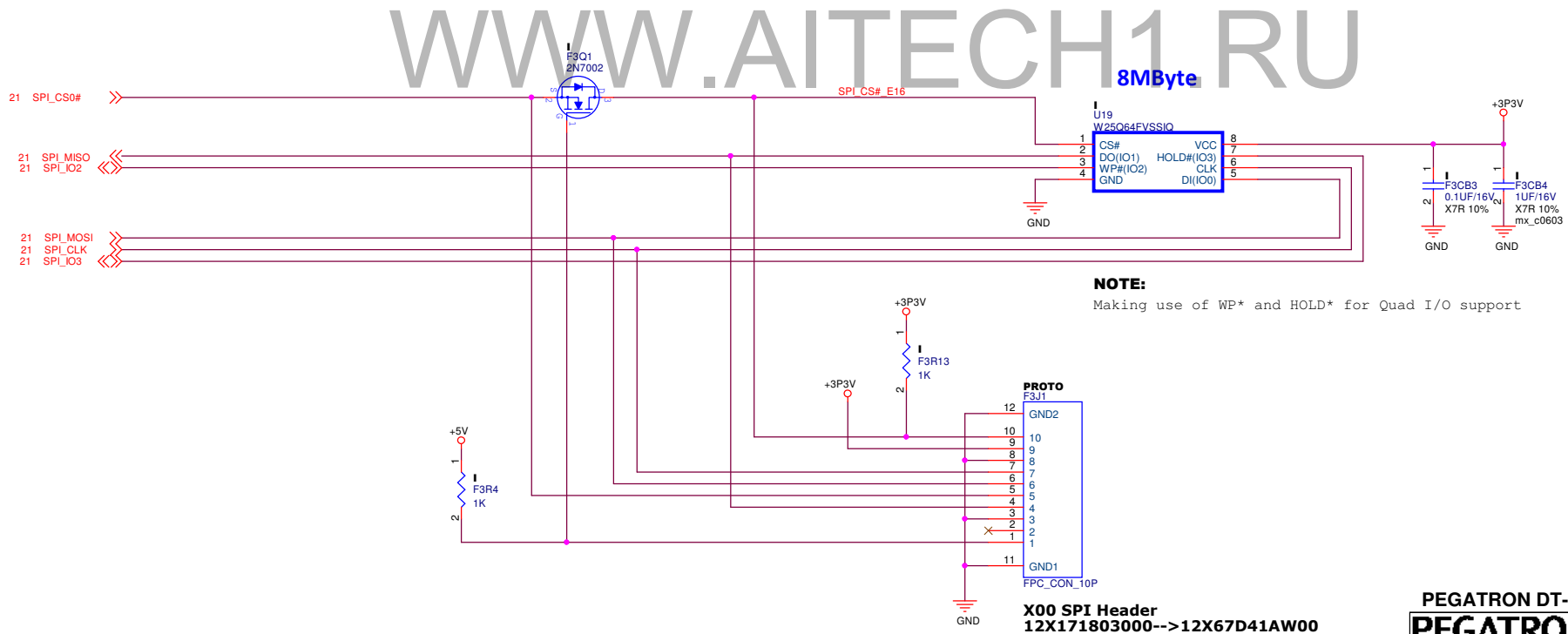
Date: Thursday, June 27, 2013

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Avoid leakage in S5



SPI ROM (Quad I/O Supported)



X00 SPI Header
12X171803000-->12X67D41AW00

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **SM BUS & SPI ROM**

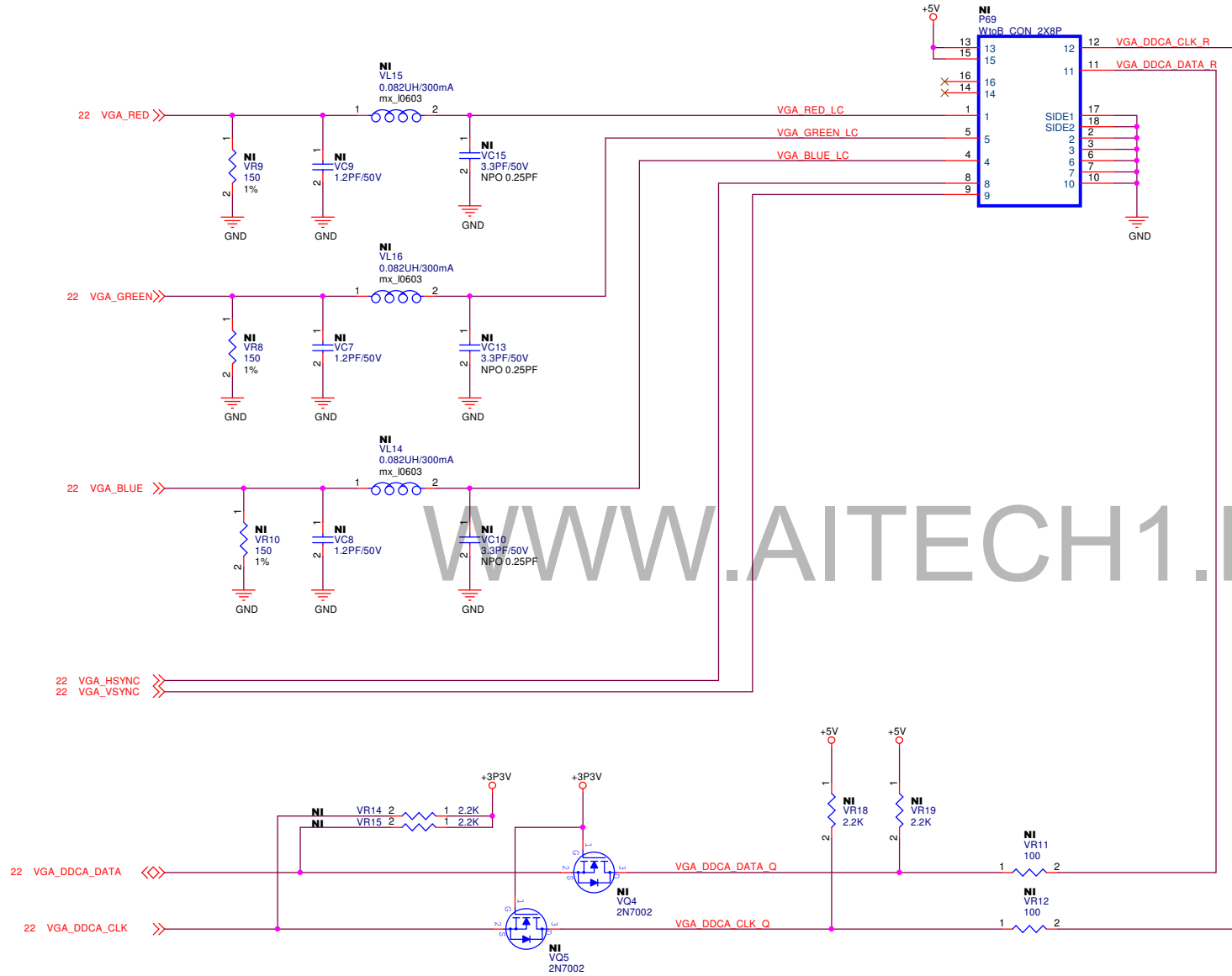
Engineer: Stonko_Chen

Size	Project Name	Rev
A0	IMPLP-MS	100

A3	IMPLP-MS			A00
Date: Thursday, June 27, 2013		Sheet	47	of 83

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X00 VGA Connector
12X341490000-->12X659528N00



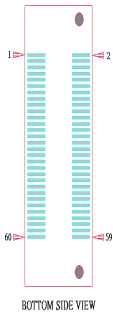
<PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **INTEGRATED VGA PORT**

Pegatron Corp. Engineer: **Stonko_Chen**

Size A3	Project Name IMPLP-MS	Rev A00
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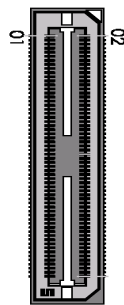
Date: Thursday, June 27, 2013 Sheet 49 of 83



BOTTOM SIDE VIEW

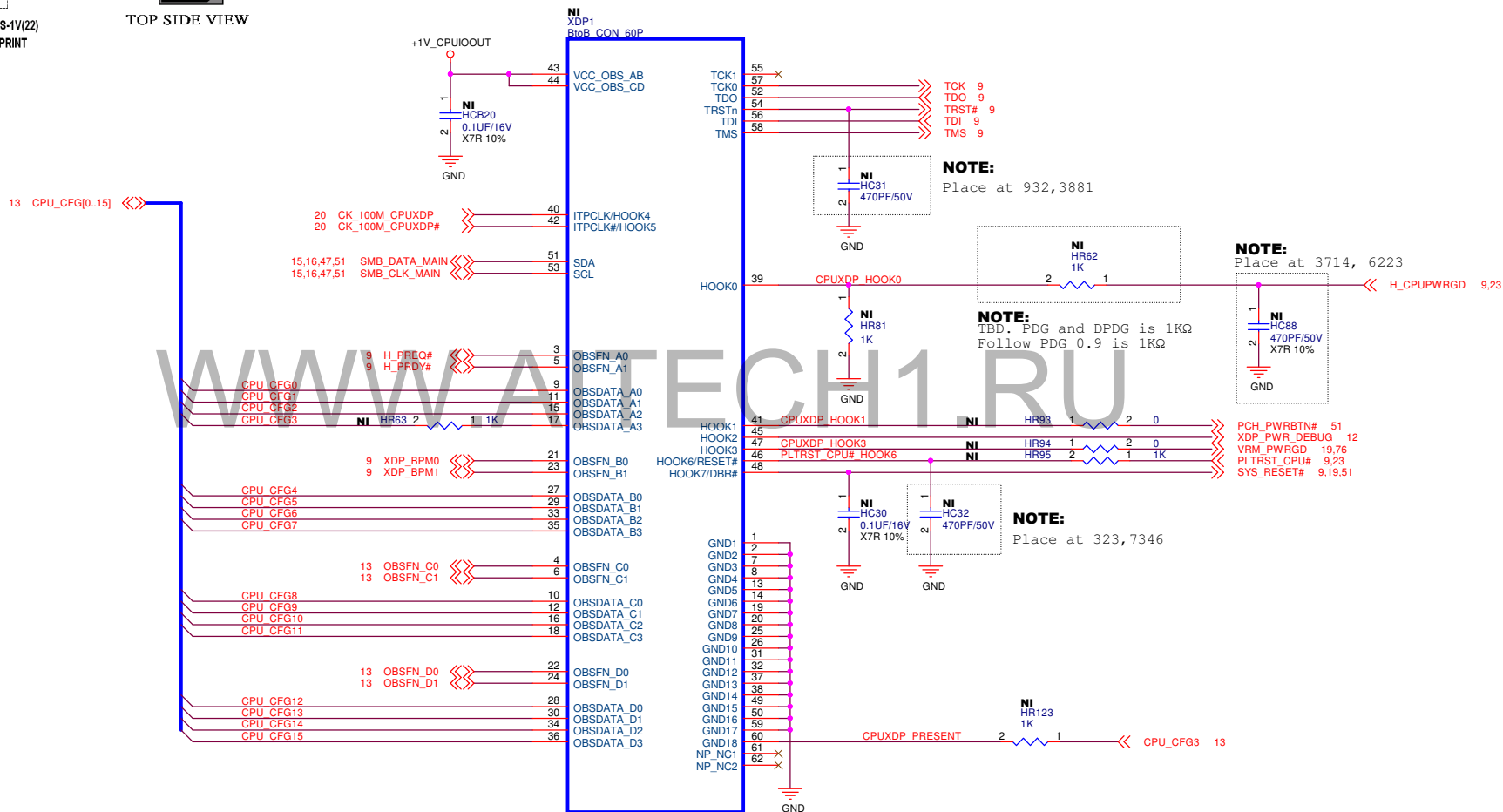


HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



TOP SIDE VIEW

INTEL CPU XDP DEBUG PORT



PEGATRON DT-MB RESTRICTED SECRET

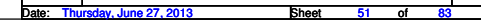
PEGATRON Title : CPU XDP DEBUG CONN.

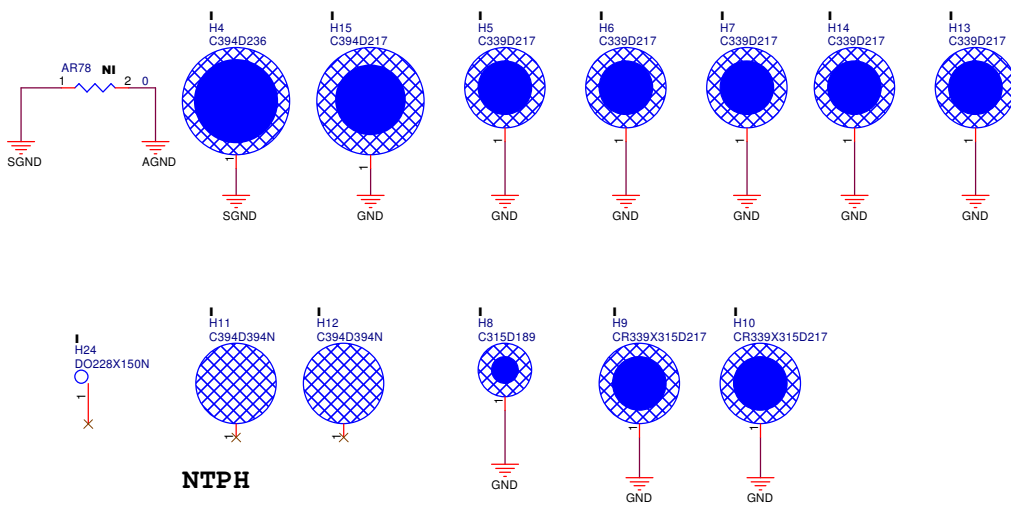
Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00

Date: Thursday, June 27, 2013 Sheet 50 of 83

Place strap resistors of TDO near to XDP connector, and TDI and TMS near to CPU.





PCB1
PCB BOARD

IMPLP-MS
PCB
Proprietary

LABEL2
PCB LABEL

BIOS
LABEL

IMPLP-MS R0.1
BOM: 69M
==> 08M1-1BL1200 (PIOTEK)
==> 08M1-1BL1000 (YUANMAO)
==> 08M1-1BL1100 (HANNSTAR)

LABEL1
PCB LABEL

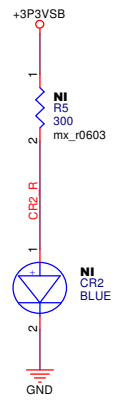
PPID LABEL

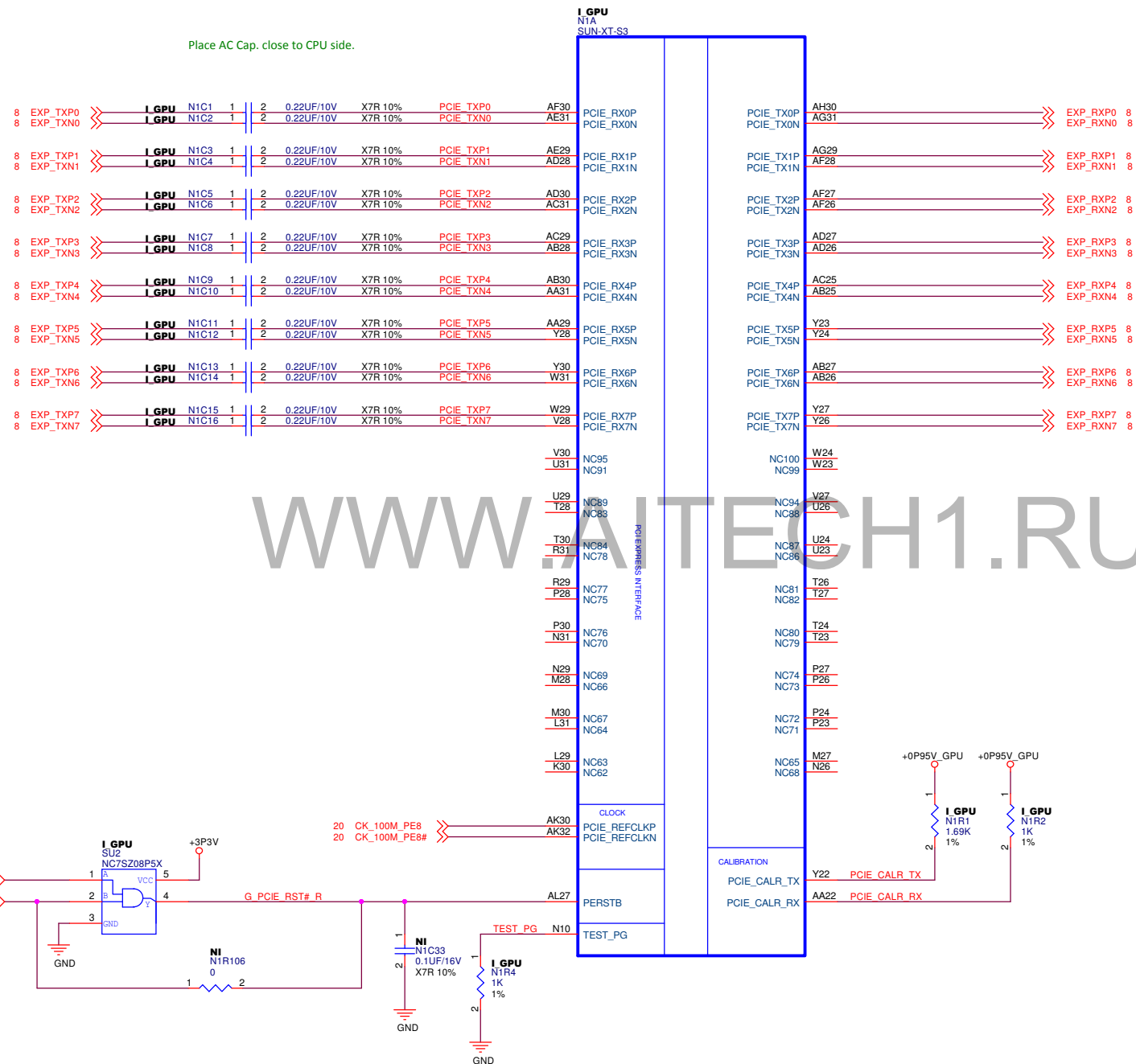
IMPLP-MS R1.00
BOM: 69M
==> 08M1-1BL0200 (PIOTEK)
==> 08M1-1BL0000 (YUANMAO)
==> 08M1-1BL0100 (HANNSTAR)

LABEL3
PCB LABEL

BLANK SN LABEL

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **SUN-XT_PCIE**

Pegatron Corp. Engineer: **Stonko_Chen**

Size A3 Project Name **IMPLP-MS** Rev A00

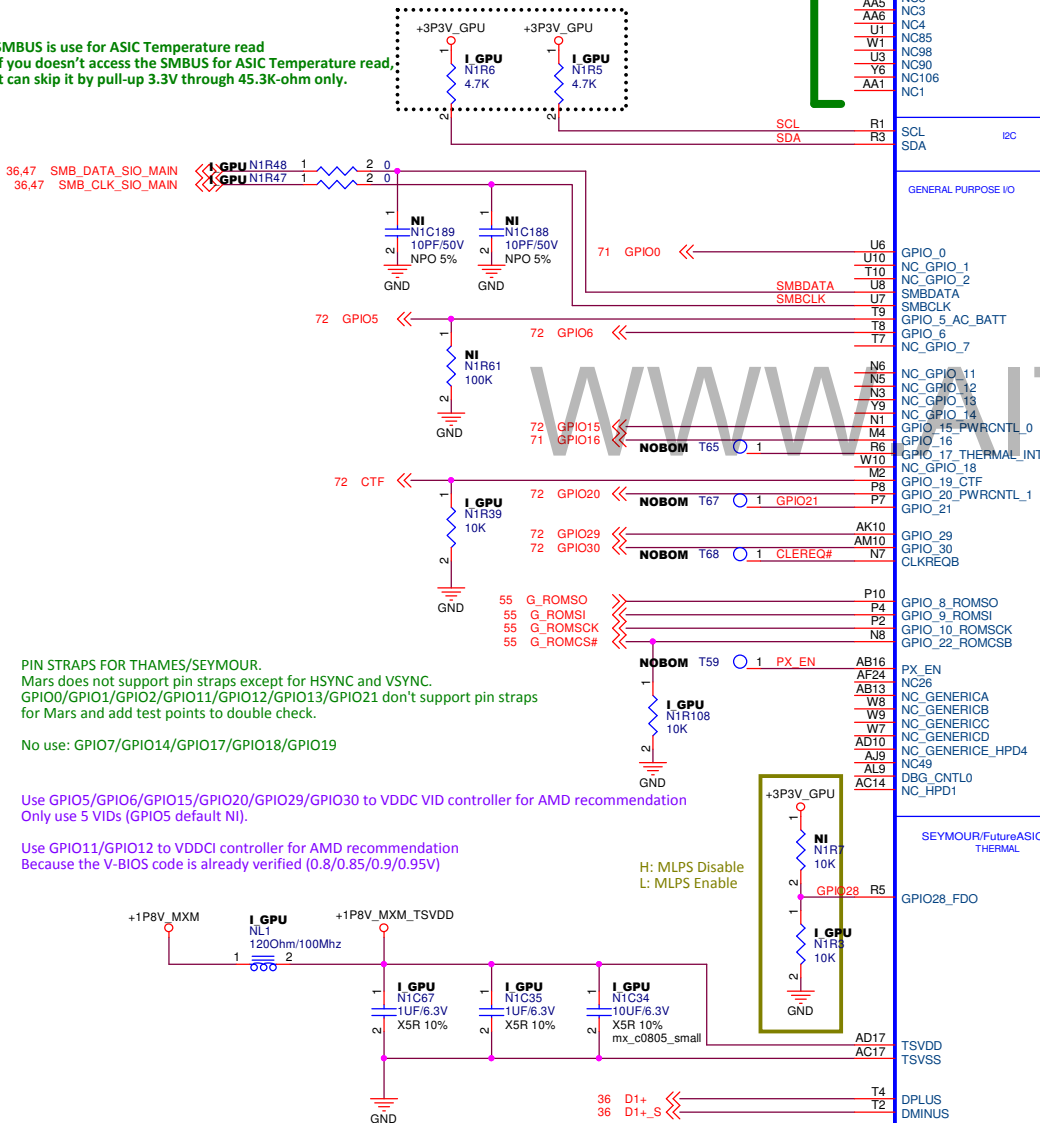
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Debug bus output data

DisplayPort Power NC for Mars-S3

Add test points on SMB Bus and SDA/SCL for debug
Access to SMB Bus ans SDA/SCL is mandatory on all designs

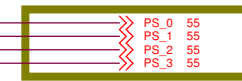
SMBUS is use for ASIC Temperature read
if you doesn't access the SMBUS for ASIC Temperature read,
it can skip it by pull-up 3.3V through 45.3K-ohm only.



DisplayPort interface For Thames/Seymour only Mars doesn't have these ports

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS
MLPS_DISABLE	NA	GPIO_P8_FSD	Enable MLPS, NA for Thames/Seymour 0: Enable MLPS, disable GPIO_PINSTRAP 1: Disable MLPS, enable GPIO_PINSTRAP
AD0(1) AD0(1)	NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

Place MLPS circuit components
as close to the ASIC PS_x balls as possible



H: Reserve Provision
L: Test Enable (Default)

Memory Type	Description
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **SUN-XT_10**

Pegatron Corp. Engineer: **Stonko_Chen**

Size **A3** Project Name **IMPLP-MS** Rev **A00**

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A



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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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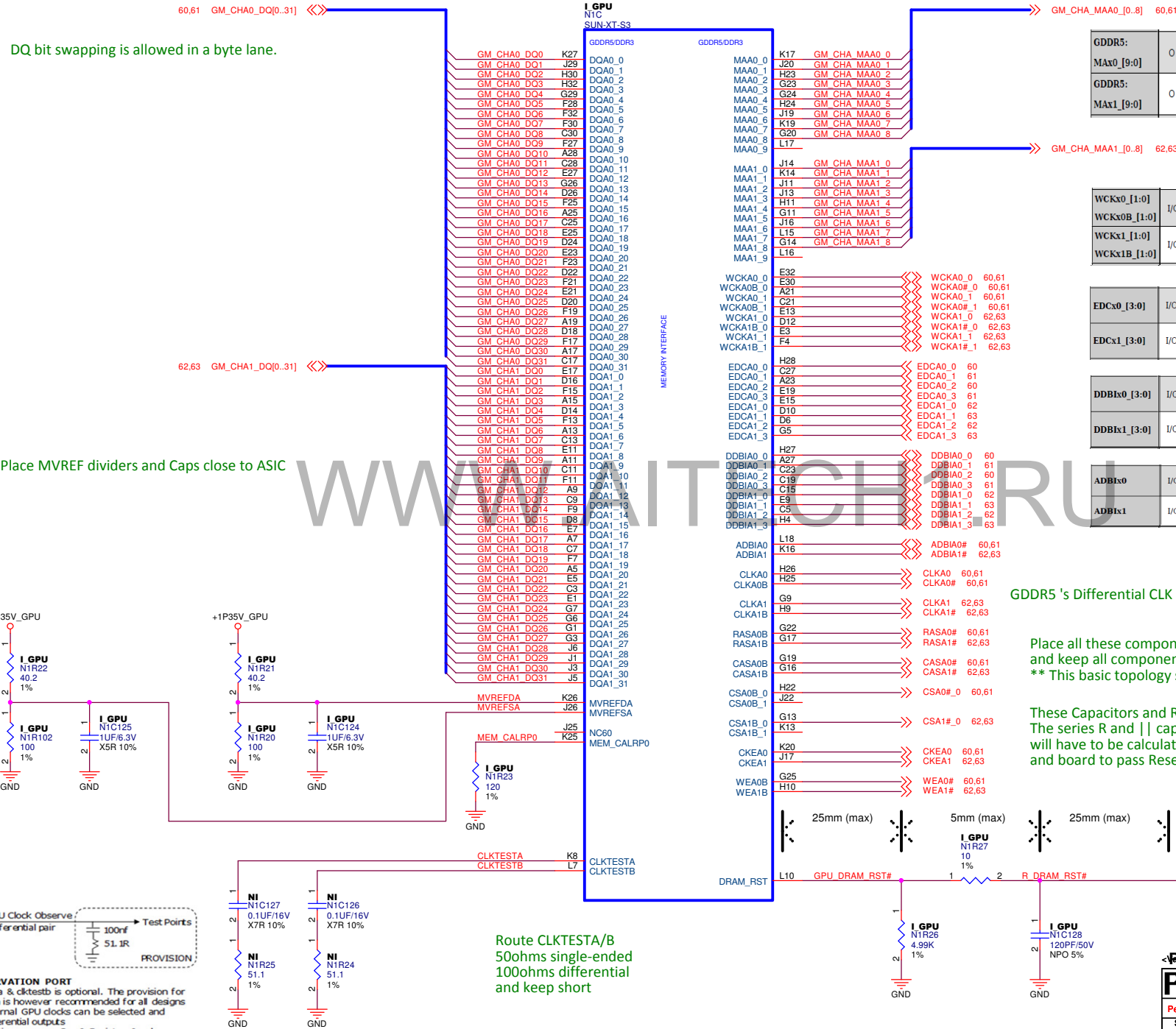
[illegible]

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[illegible]

1

MAA0_9 NC For GDDR5
MAA0_9 Connect For DDR3
MAA1_9 NC For GDDR5 & DDR3



GDDR5: Max0 [9:0]	0	GDDR5—memory address bus for channel x0. Supplies bank addresses and row/column addresses for one 32-bit interface.
GDDR5: Max1 [9:0]	0	GDDR5—memory address bus for channel x1. Supplies bank addresses and row/column addresses for one 32-bit interface.

WCKx0 [1:0]	I/O	GDDR5—forwarded clock.
WCKx0B [1:0]		DDR3—data mask for channel x0.
WCKx1 [1:0]	I/O	GDDR5—forwarded clock.
WCKx1B [1:0]		DDR3—data mask for channel x1.

EDCx0 [3:0]	I/O	GDDR5—error detection pins (input only). DDR3—differential data strobe for channel x0.
EDCx1 [3:0]	I/O	GDDR5—error detection pins (input only). DDR3—differential data strobe for channel x1.

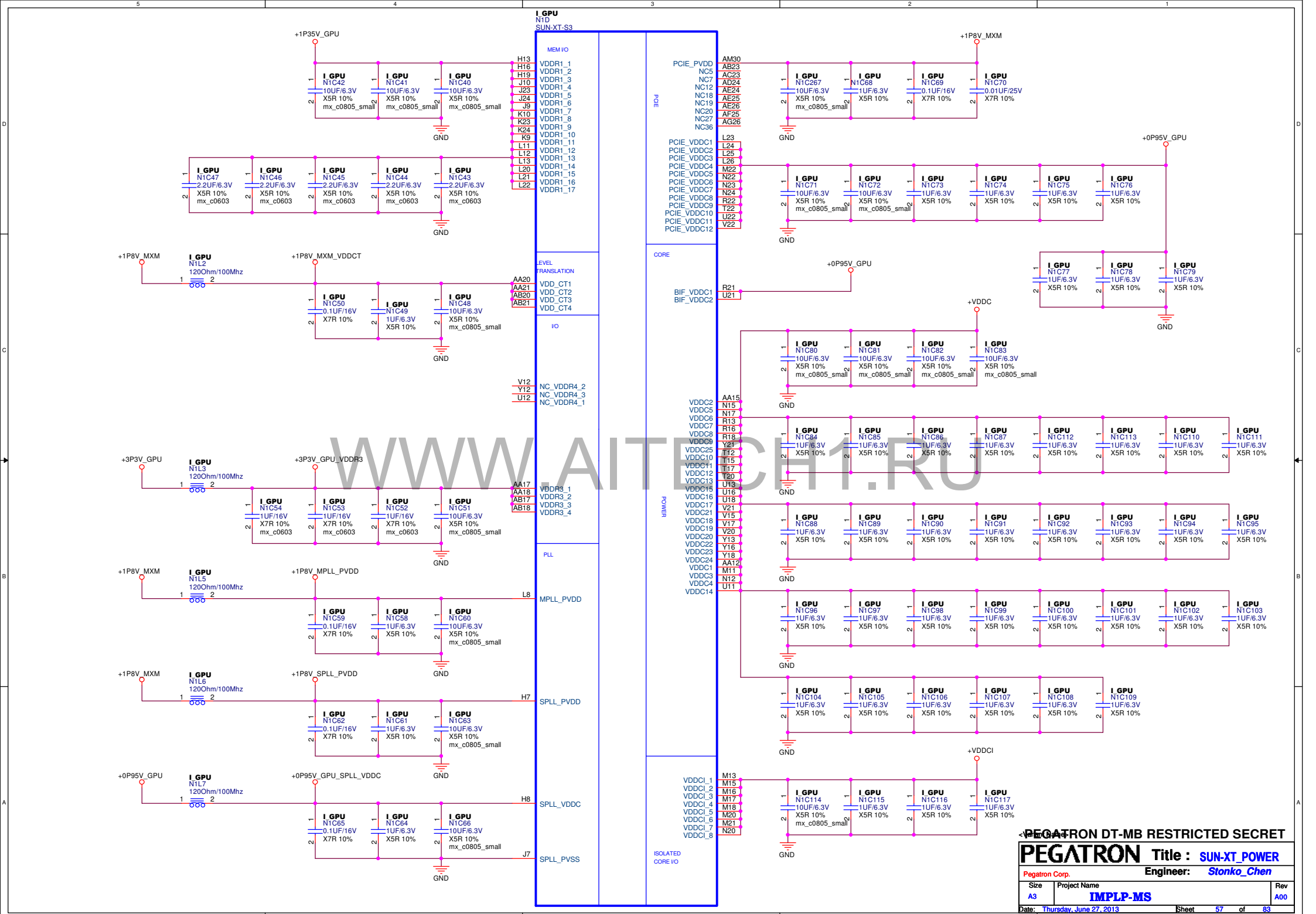
DDBIx0 [3:0]	I/O	GDDR5—data dynamic bus inversion. DDR3—differential data strobe for channel x0.
DDBIx1 [3:0]	I/O	GDDR5—data dynamic bus inversion. DDR3—differential data strobe for channel x1.

ADB1x0	I/O	GDDR5—address dynamic bus inversion for channel x0. DDR3—on-die termination control for channel x0.
ADB1x1	I/O	GDDR5—address dynamic bus inversion for channel x1. DDR3—on-die termination control for channel x1.

GDDR5 's Differential CLK signal doesn't require Clock termination using CAP.

Place all these componets very close to GPU (within 25mm)
and keep all components close to each other
** This basic topology should be used for DRAM_RAT for DDR3/GDDR5

These Capacitors and Resistor values are an example only
The series R and || cap values will depend on the DRAM loads and
will have to be calculated for different Memory, DRAM loads
and board to pass Reset Signal Spec



PEGATRON DT-MB RESTRICTED SECRET

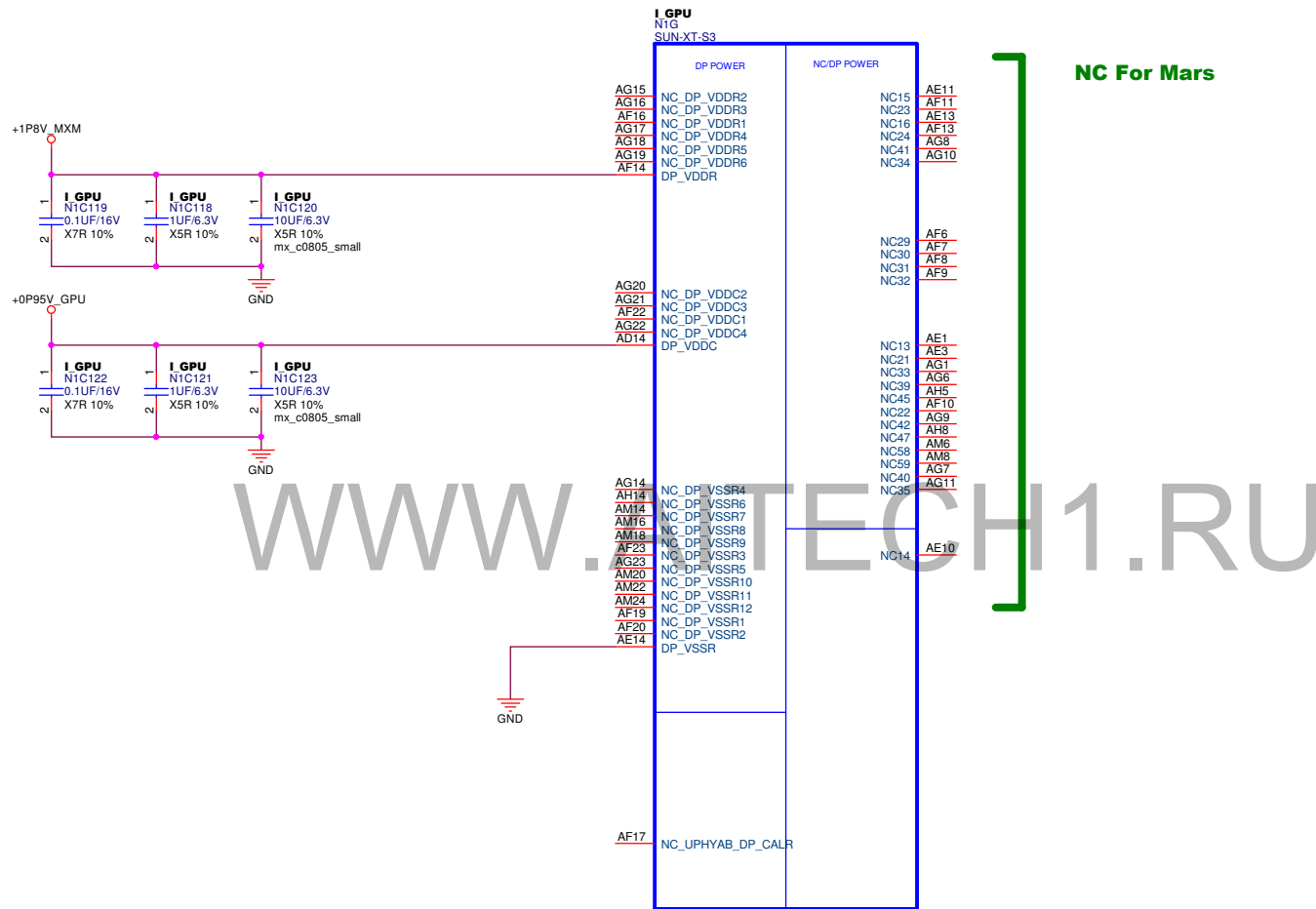
PEGATRON Title : **SUN-XT_POWER**

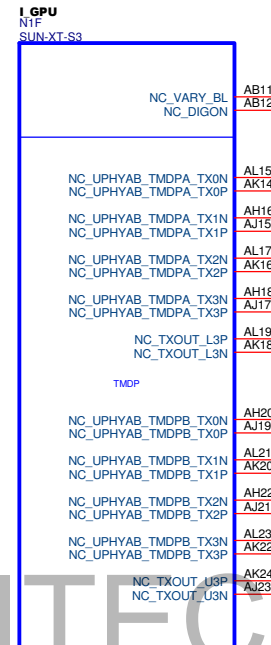
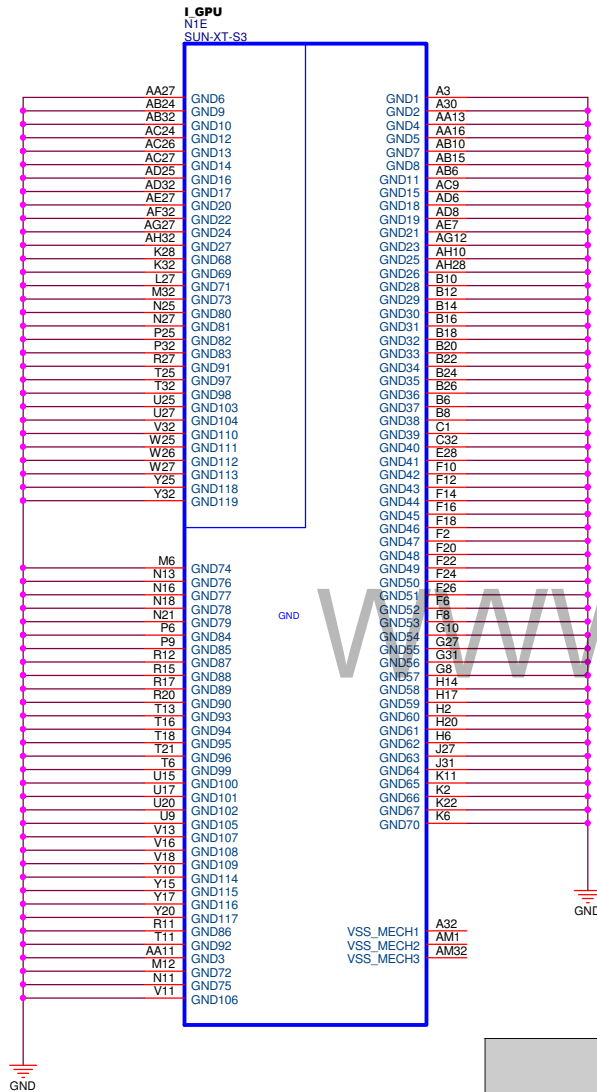
Pegatron Corp. Engineer: **Stonko_Chen**

Size A3 Project Name **IMPLP-MS** Rev A00

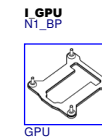
Date: Thursday, June 27, 2013 Sheet 57 of 83

Some of voltage must connect to +1.8V even though there is no used on Display feature , such as AF14 pin (DP_VDDR1) and AD14(DP_VDDC1) in SUN XT ASIC.





Mars only supports TMDPA and TMDPB

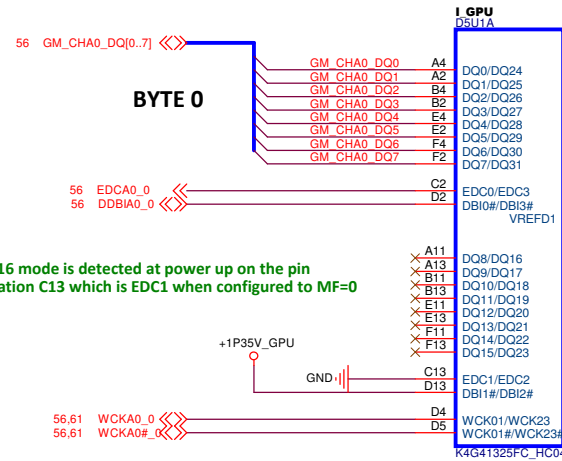


VSS_MECH	Gnd	<p>The primary purpose of these balls is to provide additional mechanical strength between the ASIC and PCB. The PCB pads for the VSS_MECH balls should not be connected (NC) on the PCB.</p> <p>VSS_MECH balls are electrically connected to the ASIC's ground plane (VSS), however, they are not needed as ground signals.</p>
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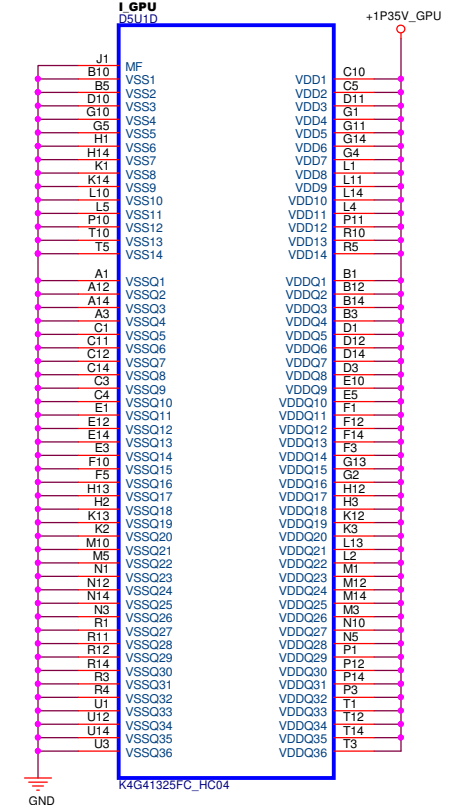
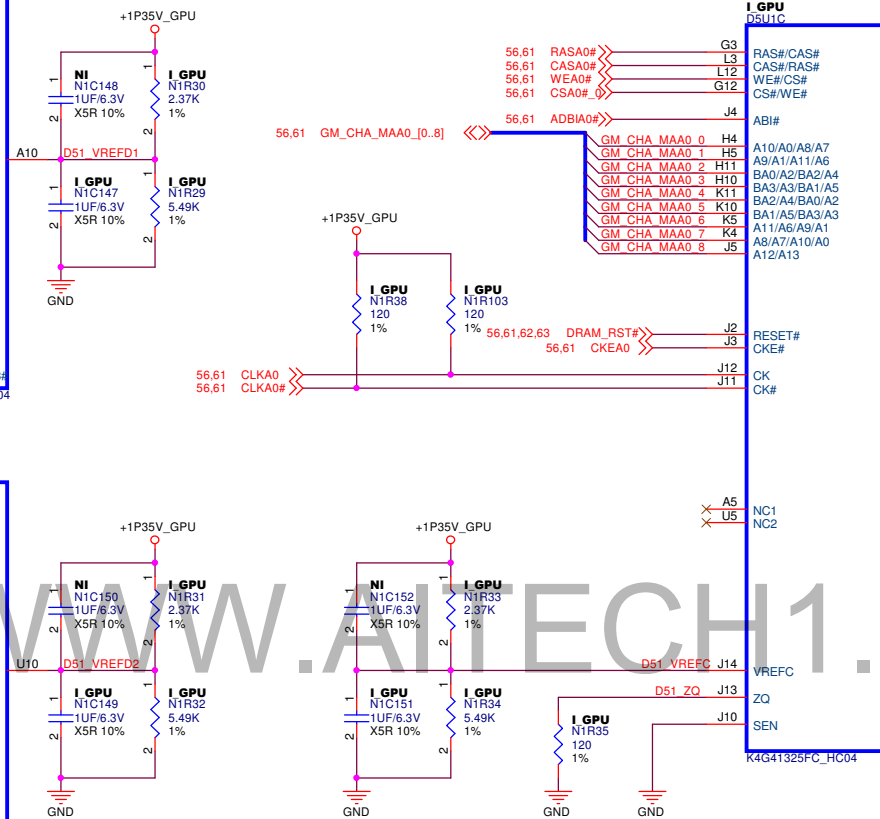
CELL1 TOP X16 MODE (MF=0)

GDDR5
HYNIX 0315-011A0DE
Samsung 0315-010U0DE

MF=0



The x16 mode is detected at power up on the pin at location C13 which is EDC1 when configured to MF=0



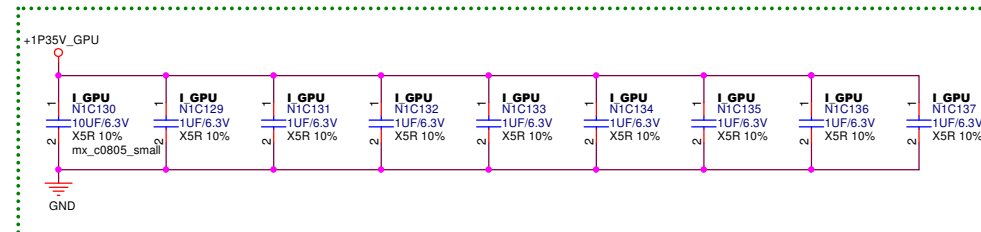
Decoupling caps for clamshell configuration (2 chip at top and bottom)

1 X 10uf per 2 clamshell DRAMs

8 X 1uf per 2 clamshell DRAMs

Note: it is recommended to use a clamshell placement of the two QDR II SRAM components to achieve minimal stub delays and optimum signal integrity.

Clamshell placement is when two devices overlay each other by being placed on opposite sides of the PCB.



Note: Stitching Caps OPTION for MEM signals that have a change of reference plane voltage
Add stitching caps when required, one cap per three signals

<Variant Name> REGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GDDR5 X16 XCELL1_TOP

Pegatron Corp. **Engineer:** *Stonko_Chen*

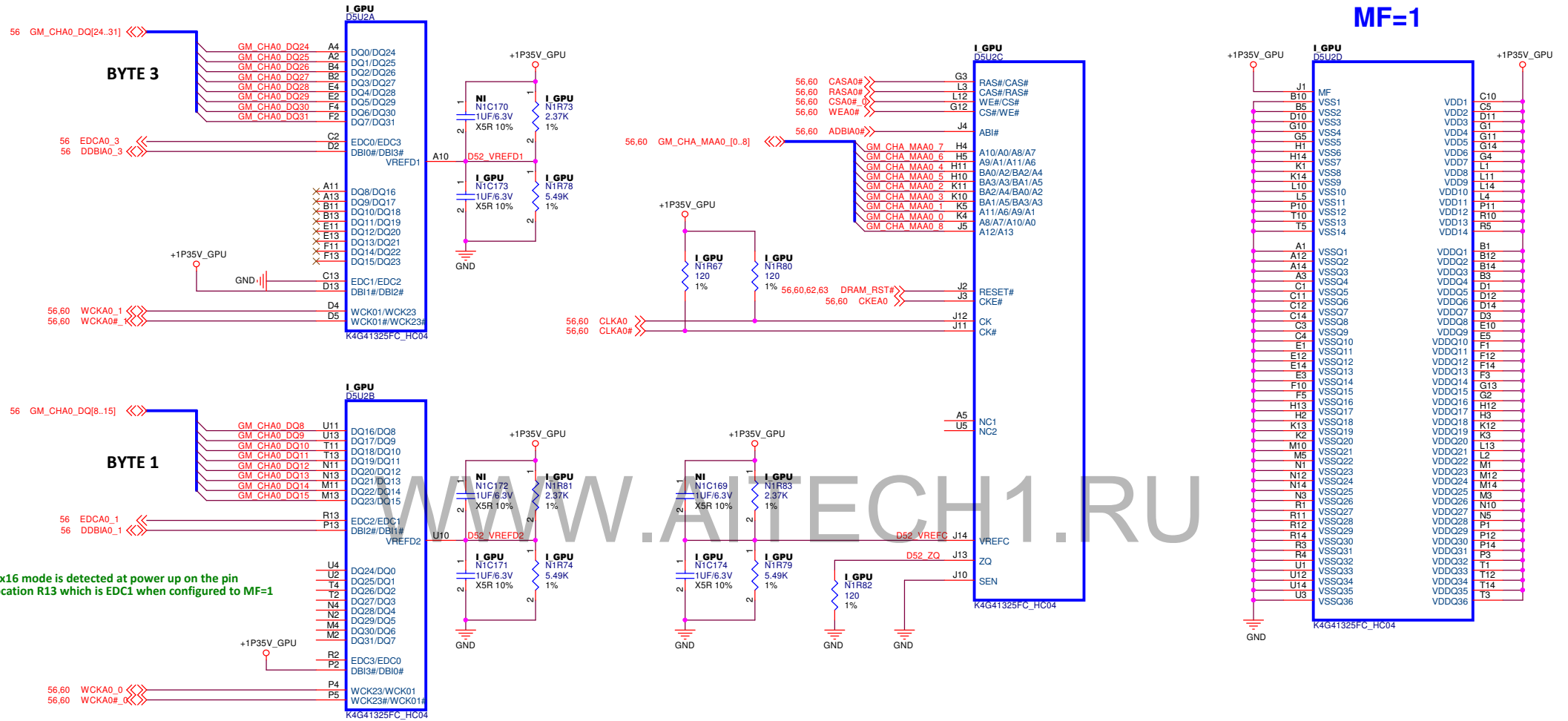
Size	Project Name	Rev
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A3	IMPLP-MS	A00
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Date: Thursday, June 27, 2013 Sheet 60 of 83

CELL1 BOTTOM X16 MODE (MF=1)

MF=1



The x16 mode is detected at power up on the pin at location R13 which is EDC1 when configured to MF=1

MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=1, RAS# / CAS# / WE# / CS# / ADDRESS will mirror.	
DQ0	DQ24	WCK01/01#	WCK23/23#	A0	A7	MF=0	MF=1
DQ1	DQ25	WCK23/23#	WCK01/01#	A1	A6	RAS#	CAS#
DQ2	DQ26	DBI0#	DBI3#	A2	A4	CAS#	RAS#
DQ3	DQ27	DBI1#	DBI2#	A3	A5	CS#	WE#
DQ4	DQ28	DBI2#	DBI1#	A4	A2	WE#	CS#
DQ5	DQ29	DBI3#	DBI0#	A5	A3		
DQ6	DQ30	EDC0	EDC3	A6	A1		
DQ7	DQ31	EDC1	EDC2	A7	A0		
		EDC2	EDC1				
		EDC3	EDC0				
DQ16	DQ8						
DQ17	DQ9						
DQ18	DQ10						
DQ19	DQ11						
DQ20	DQ12						
DQ21	DQ13						
DQ22	DQ14						
DQ23	DQ15						

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GDDR5 X16 XCELL1_BOT

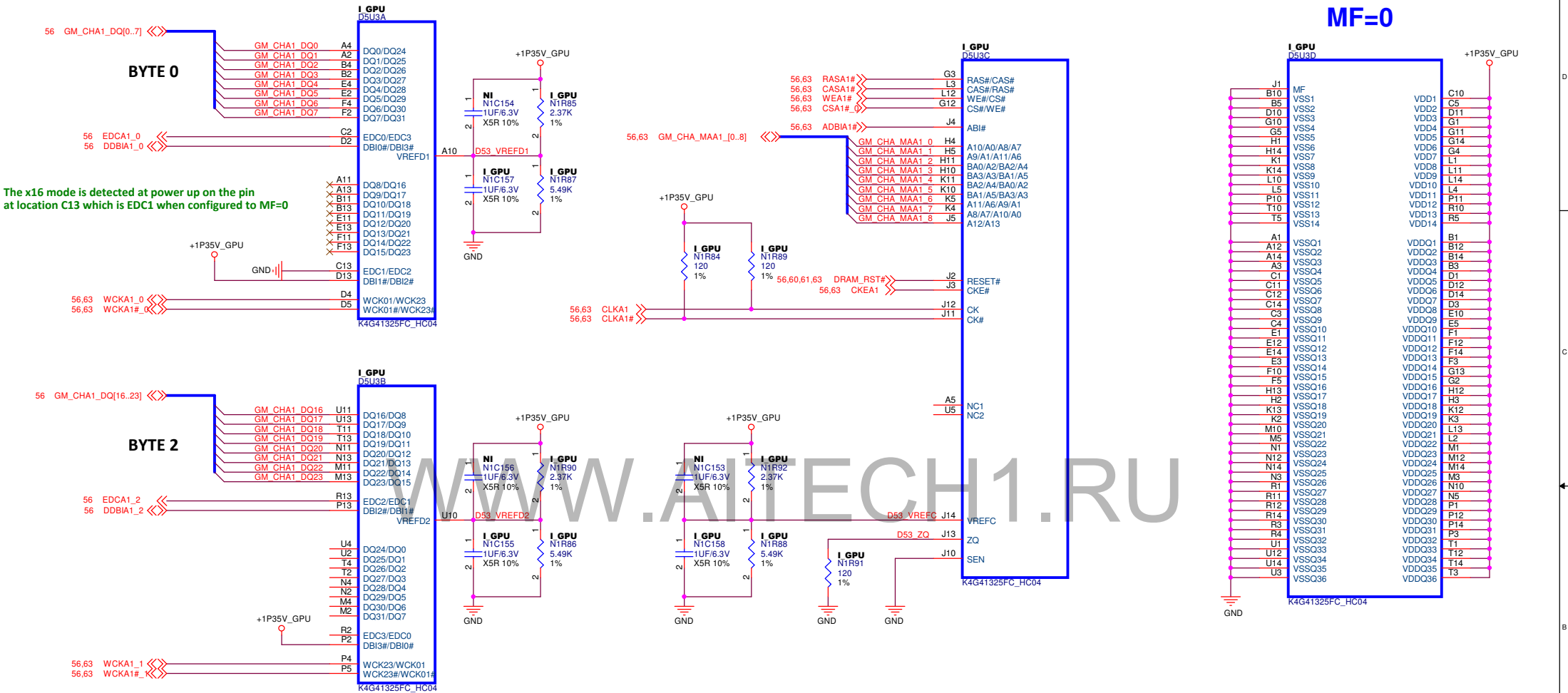
Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00

Date: Thursday, June 27, 2013 Sheet 61 of 83

CELL2 TOP X16 MODE (MF=0)

MF=0

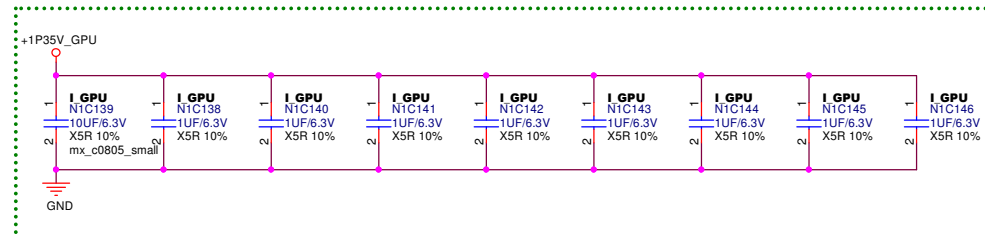


Decoupling caps for clamshell configuration (2 chip at top and bottom)

1 X 10uf per 2 clamshell DRAMs

8 X 1uf per 2 clamshell DRAMs

Note: it is recommended to use a clamshell placement of the two QDR II SRAM components to achieve minimal stub delays and optimum signal integrity. Clamshell placement is when two devices overlay each other by being placed on opposite sides of the PCB.



Note: Stitching Caps OPTION for MEM signals that have a change of reference plane voltage
Add stitching caps when required, one cap per three signals

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GDDR5 X16 XCELL2_TOP

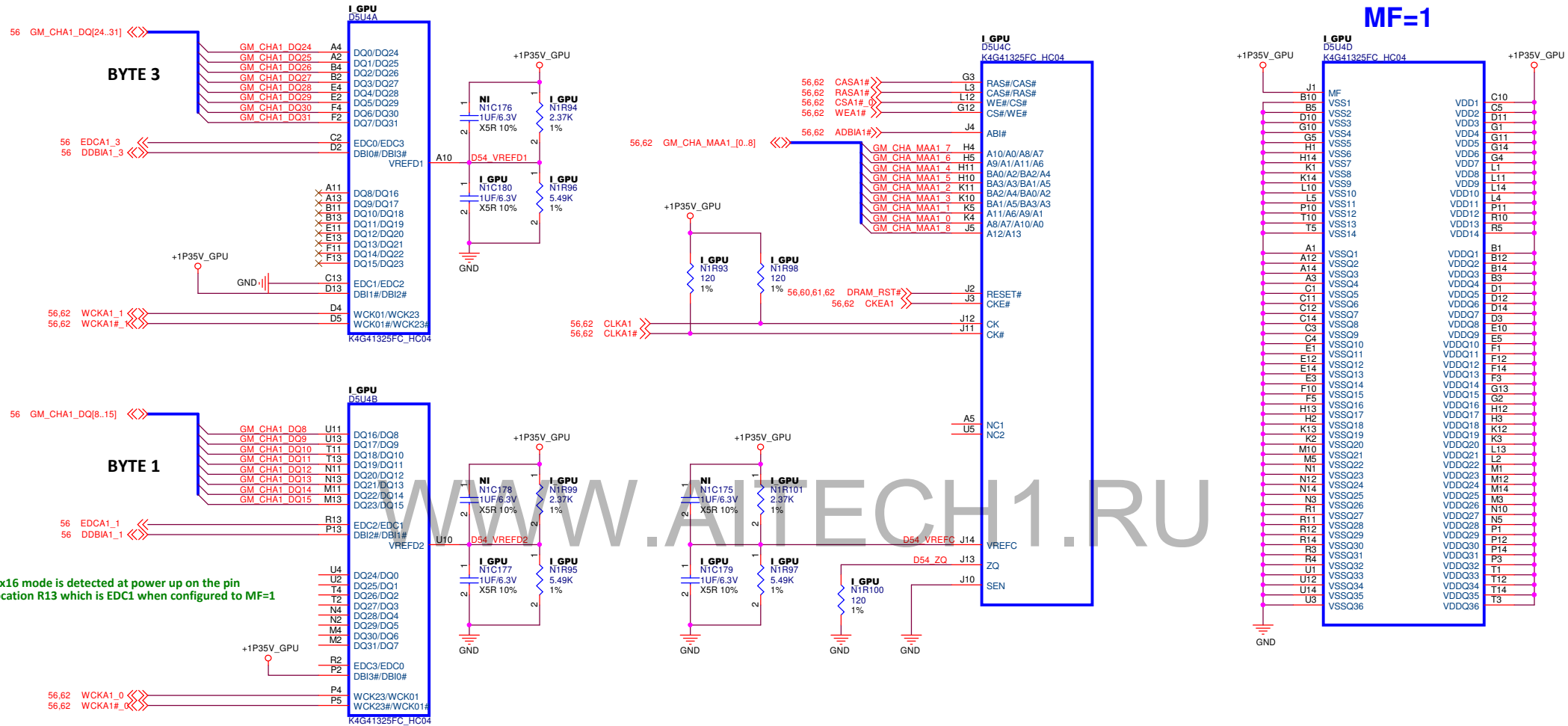
Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name IMPLP-MS Rev A00

Date: Thursday, June 27, 2013 Sheet 62 of 83

CELL2 BOTTOM X16 MODE (MF=1)

MF=1



The x16 mode is detected at power up on the pin at location R13 which is EDC1 when configured to MF=1

MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=1 , RAS# / CAS# / WE# / CS# / ADDRESS will mirror	
DQ0	DQ24	WCK01/01#	WCK23/23#	A0	A7	MF=0	MF=1
DQ1	DQ25	WCK23/23#	WCK01/01#	A1	A6	RAS#	CAS#
DQ2	DQ26	DBI0#	DBI3#	A2	A4	CAS#	RAS#
DQ3	DQ27	DBI1#	DBI2#	A3	A5	CS#	WE#
DQ4	DQ28	DBI2#	DBI1#	A4	A2	WE#	CS#
DQ5	DQ29	DBI3#	DBI0#	A5	A3		
DQ6	DQ30	EDC0	EDC3	A6	A1		
DQ7	DQ31	EDC1	EDC2	A7	A0		
		EDC2	EDC1				
		EDC3	EDC0				
DQ16	DQ8						
DQ17	DQ9						
DQ18	DQ10						
DQ19	DQ11						
DQ20	DQ12						
DQ21	DQ13						
DQ22	DQ14						
DQ23	DQ15						

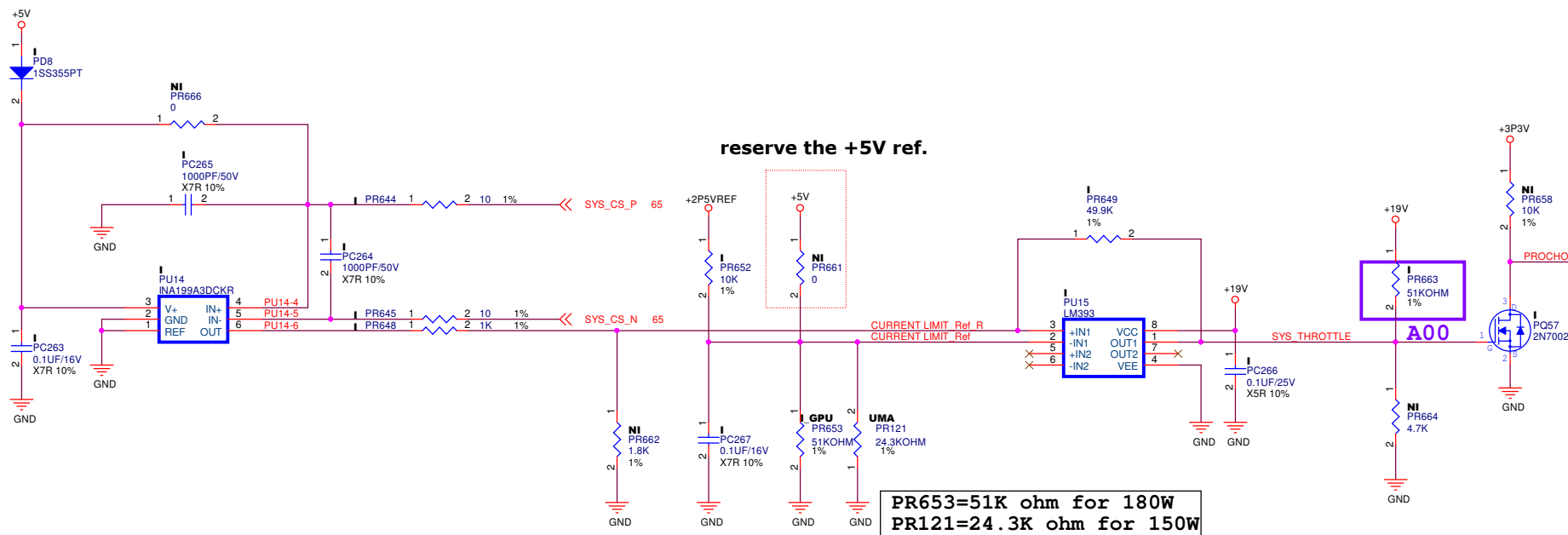
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GDDR5 X16 CELL2_BOT

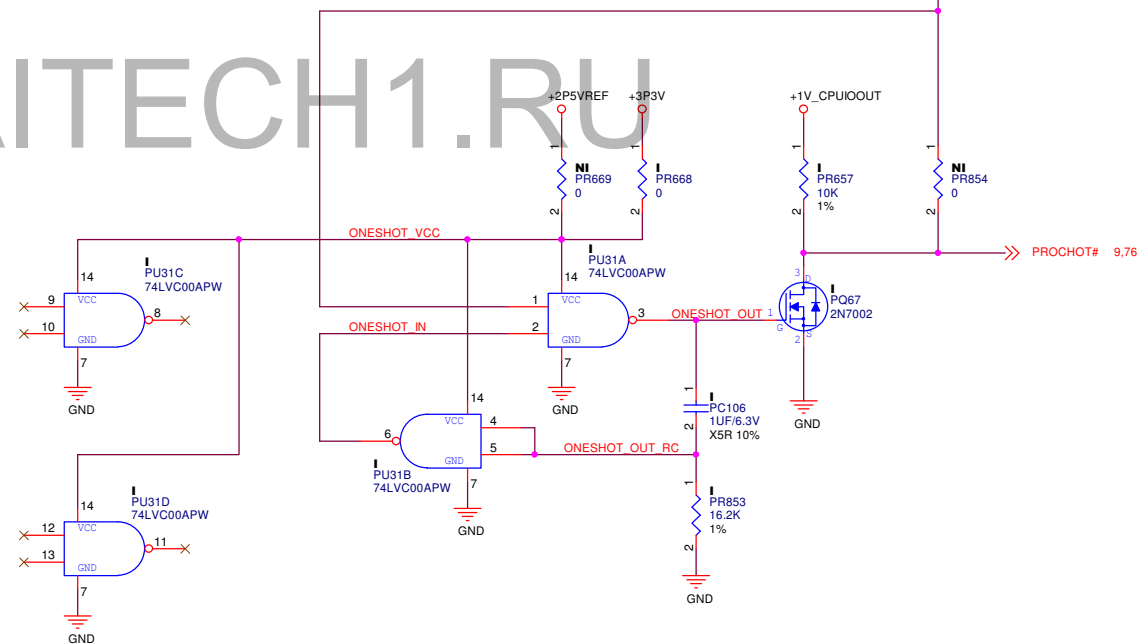
Pegatron Corp. Engineer: Stonko_Chen

Size	Project Name	Rev
A3	IMPLP-MS	A00

Date: Thursday, June 27, 2013 Sheet 63 of 83



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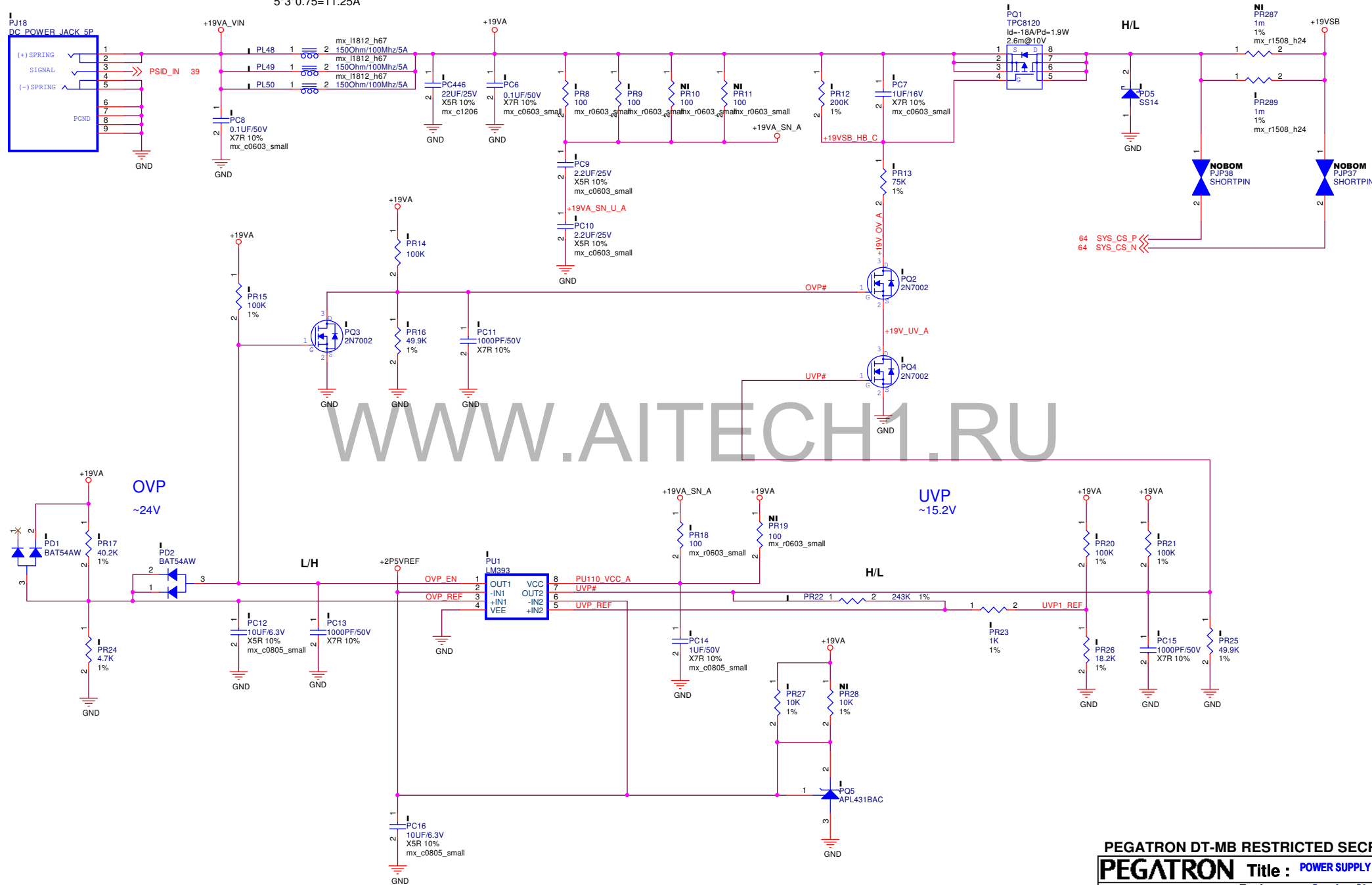
PROCHOT# One shot circuit

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **CURRENT LIMIT**
Pegatron Corp. Engineer: **Stonko_Chen**

Size	Project Name	Rev
A3	IMPLP-MS	A00
Date: Thursday, June 27, 2013	Sheet 64 of 83	

180/19.5=9.23A
5*3*0.75=11.25A



PEGATRON DT-MB RESTRICTED SECRET

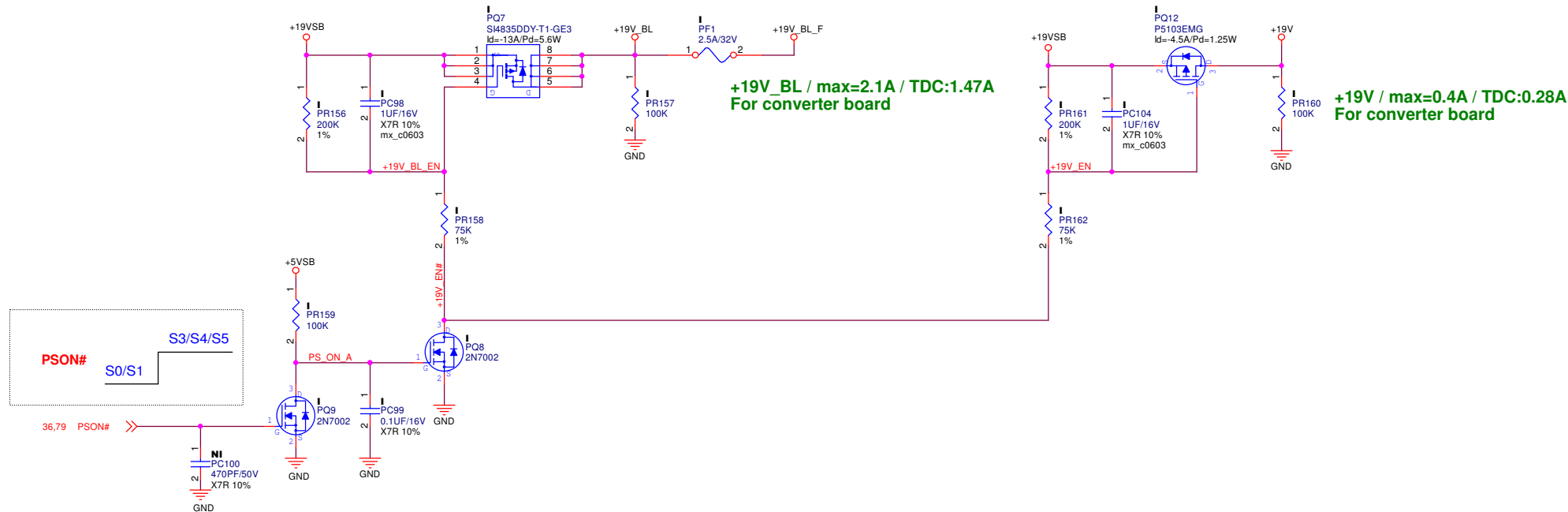
PEGATRON Title : POWER SUPPLY VIN

Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name

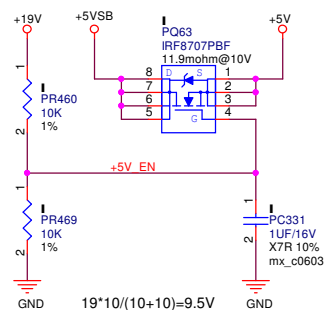
Rev A00

Date: Thursday, June 27, 2013 Sheet 65 of 83



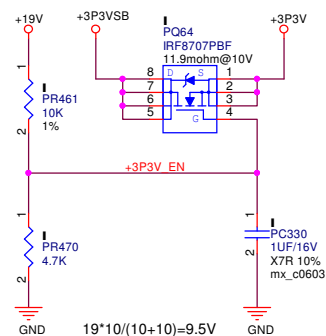
+5V/Imax:3.5A/TDC:2.45A

$5-3.5 \times 11.9\text{m} = 4.95835\text{V} > 5 \times 0.95 = 4.75\text{V}$
 $V_{\text{droop}} = 3.5\text{A} \times 11.9\text{mohm} = 41.65\text{mV}$
 $P_d = 3.5 \times 2 \times 11.9\text{m} = 145.775\text{mW}$



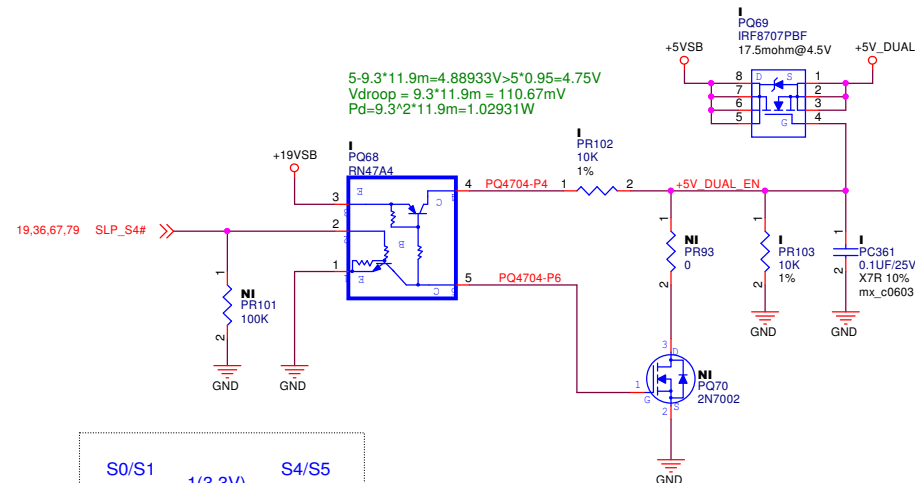
+3P3V / max:2.552A / TDC:1.786A

$3-11.9 \times 2.552\text{m} = 2.97\text{V} > 3 \times 0.95 = 2.85\text{V}$
 $V_{\text{droop}} = 2.552\text{A} \times 11.9\text{mohm} = 30.3688\text{mV}$
 $P_d = 2.552 \times 2 \times 11.9\text{m} = 77.5\text{mW}$



+5V_DUAL / Imax=9.3A/TDC=6.5A

$5-9.3 \times 11.9\text{m} = 4.88933\text{V} > 5 \times 0.95 = 4.75\text{V}$
 $V_{\text{droop}} = 9.3 \times 11.9\text{m} = 110.67\text{mV}$
 $P_d = 9.3 \times 2 \times 11.9\text{m} = 1.02931\text{W}$



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +5V_DUAL / +5V / +3P3V

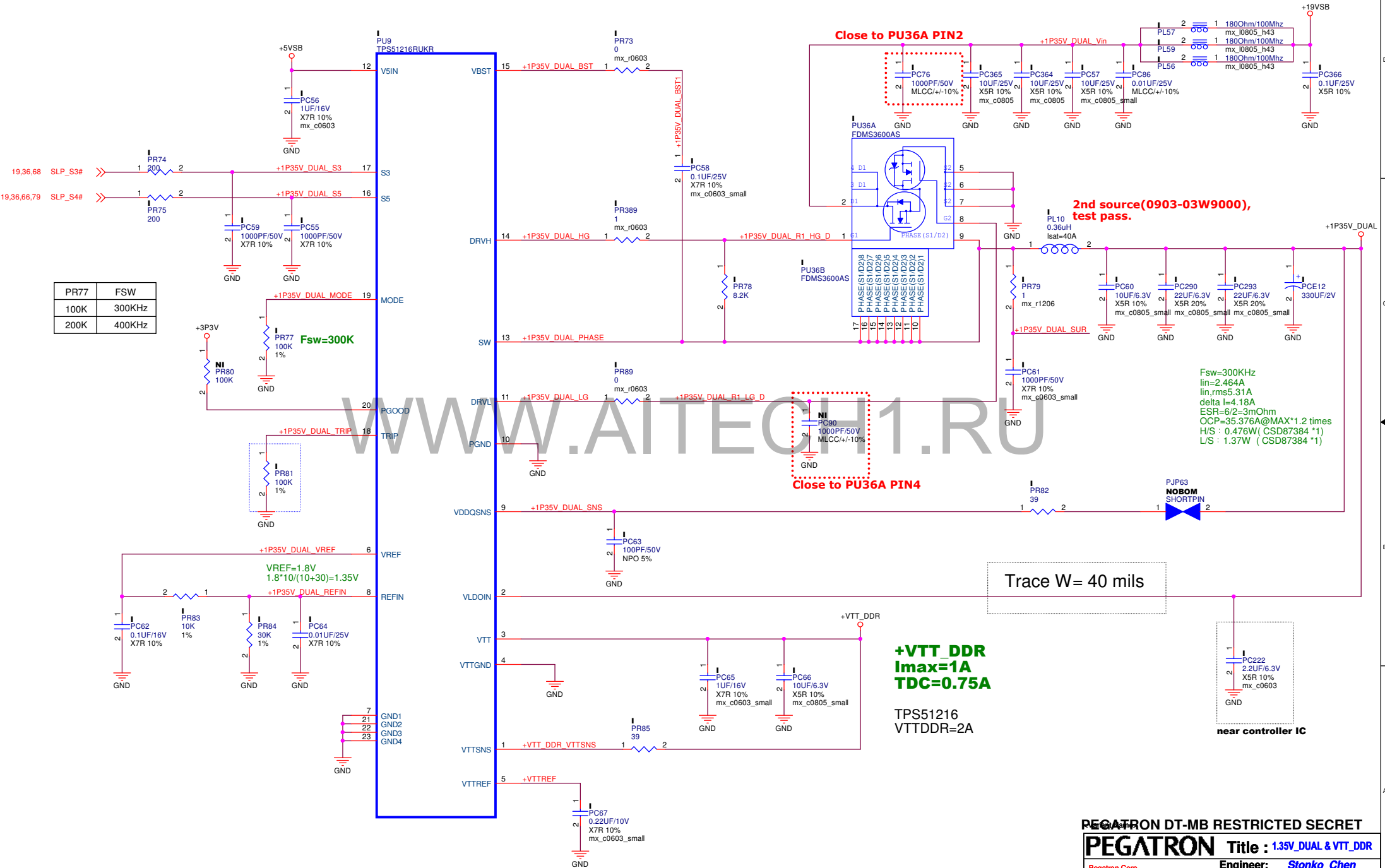
Pegatron Corp. Engineer: **Stonko_Chen**

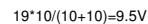
Size A3 Project Name **IMPLP-MS** Rev A00

Date: Thursday, June 27, 2013 Sheet 66 of 83

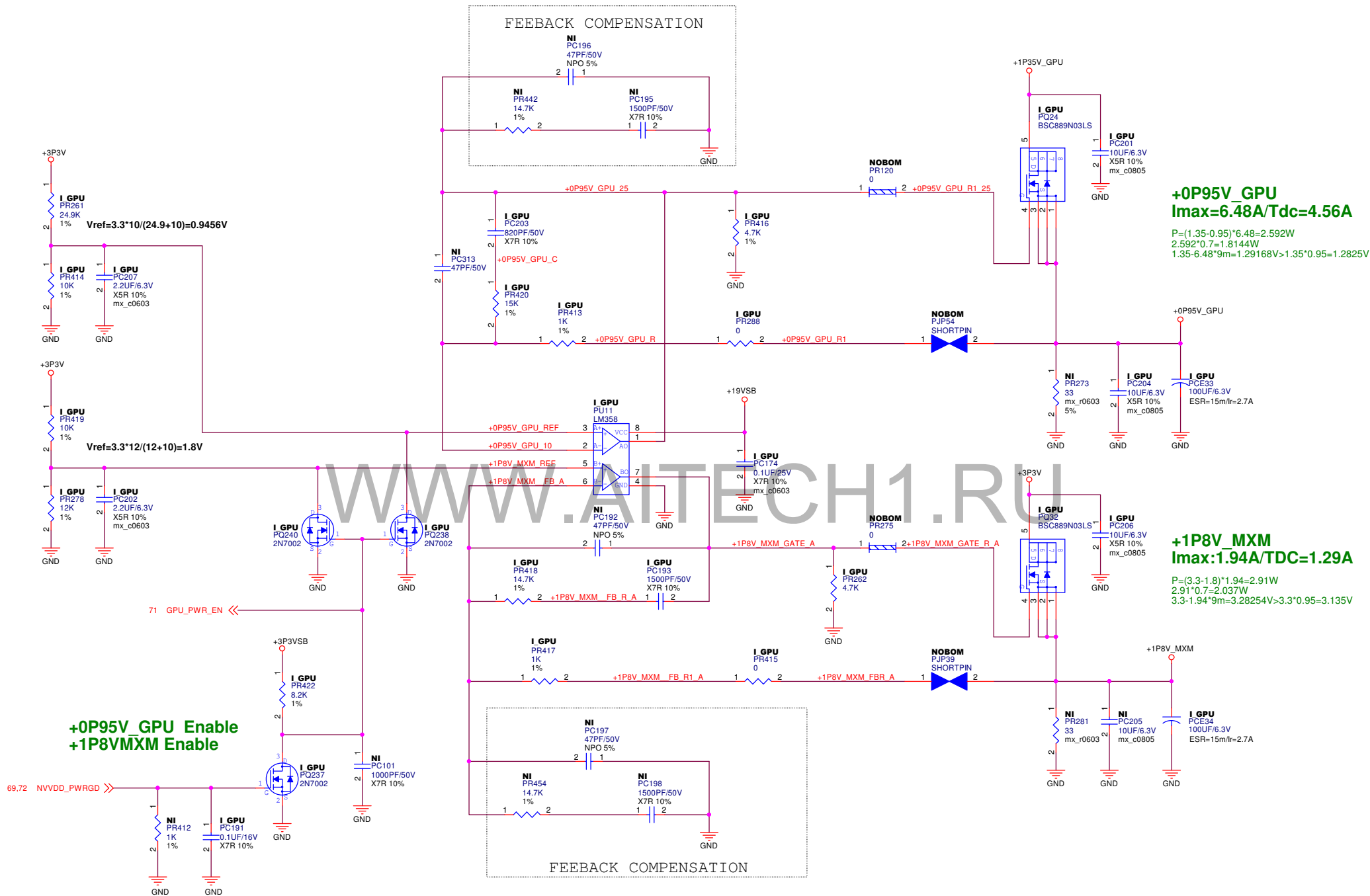
+1P35V_DUAL
Imax=29.48A(12.57+1.43A DDR+9A VDDCI+6.48A 0P95GPU)
TDC=20.636A

PR77	FSW
100K	300KHz
200K	400KHz





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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P8V & 0P95V_GPU

Pegatron Corp. Engineer: Stonko_Chen

Size A3	Project Name IMPLP-MS	Rev A00
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Date: Thursday, June 27, 2013 Sheet 70 of 83

FEEDBACK COMPENSATION

$$V_{ref} = 3.3 \times 8.45 / (8.45 + 12.1) = 1.3569V$$

PU ON PCH SIDE

GPI00	GPI016	VDDCI
0	0	0.95V
0	1	0.9V
1	0	0.85V
1	1	0.8V

+1P35V_GPU
 $I_{max} = 8.77A / TDC = 6.14A$
 $P = (1.5 - 1.35) \times 8.77 = 1.3155W$
 $1.3155 \times 0.7 = 0.92085W$
 $1.5 - 8.77 \times 9m = 1.42107V > 1.5 \times 0.95 = 1.425V$

+VDDCI/1.15V
 $I_{max} = 9A / TDC = 6A$
 $P = (1.35 - 1.15) \times 9 = 1.8W$
 $1.8 \times 0.7 = 1.26W$
 $1.35 - 9 \times (9m/2) = 1.3095V > 1.35 \times 0.95 = 1.2825V$

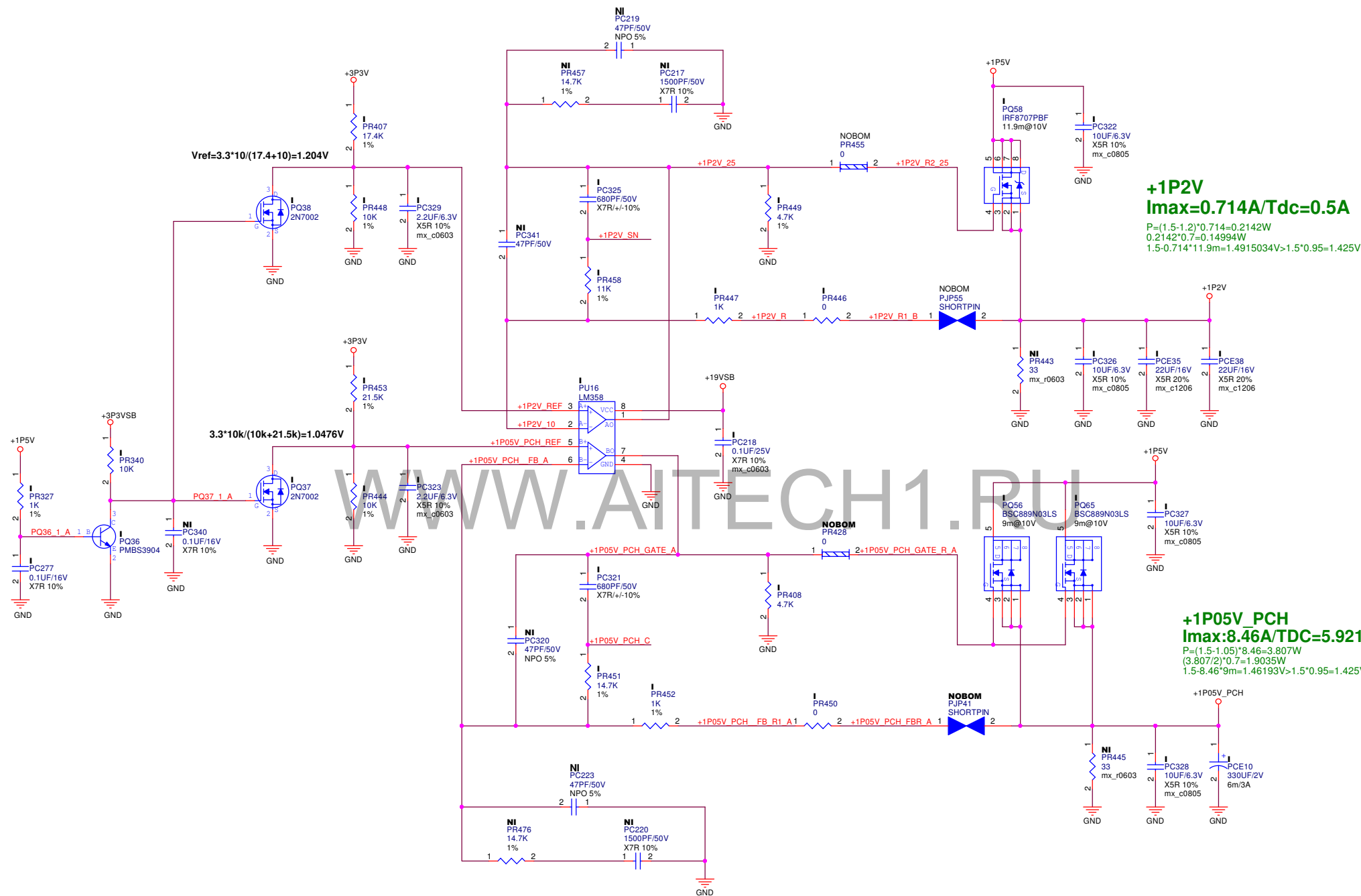
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 1P35VGPU&VDDCI

Pegatron Corp. Engineer: Stonko_Chen

Size A3 Project Name **IMPLP-MS** Rev A00

Date: Thursday, June 27, 2013 Sheet 71 of 83



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P2V & +1P8V_MXM

Pegatron Corp. Engineer: Stonko_Chen

Size A3	Project Name IMPLP-MS	Rev A00
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+5VA
IMAX=0.1A
TDC=0.07A

+3P3VA
IMAX=0.101A
TDC=0.0707A

+5VSB Fsw=300K
+3V3PSB Fsw=350K

OCP_5V=12.8*1.4=17.92A
delta l=3.72A, Rds(on)=9mOhm,
Vtrip=(17.92-3.72/2)*8*9m=1.156269V
Rtrip=Vtrip/Itrip=1.156269/10^-6=115.6K

OCP_3V=8.325*1.4=11.655A
delta l=2.33A, Rds(on)=9m
Vtrip=(11.655-2.33/2)*8*9m=0.755365V
Rtrip=Vtrip/Itrip=0.755365/10^-6=75.5K

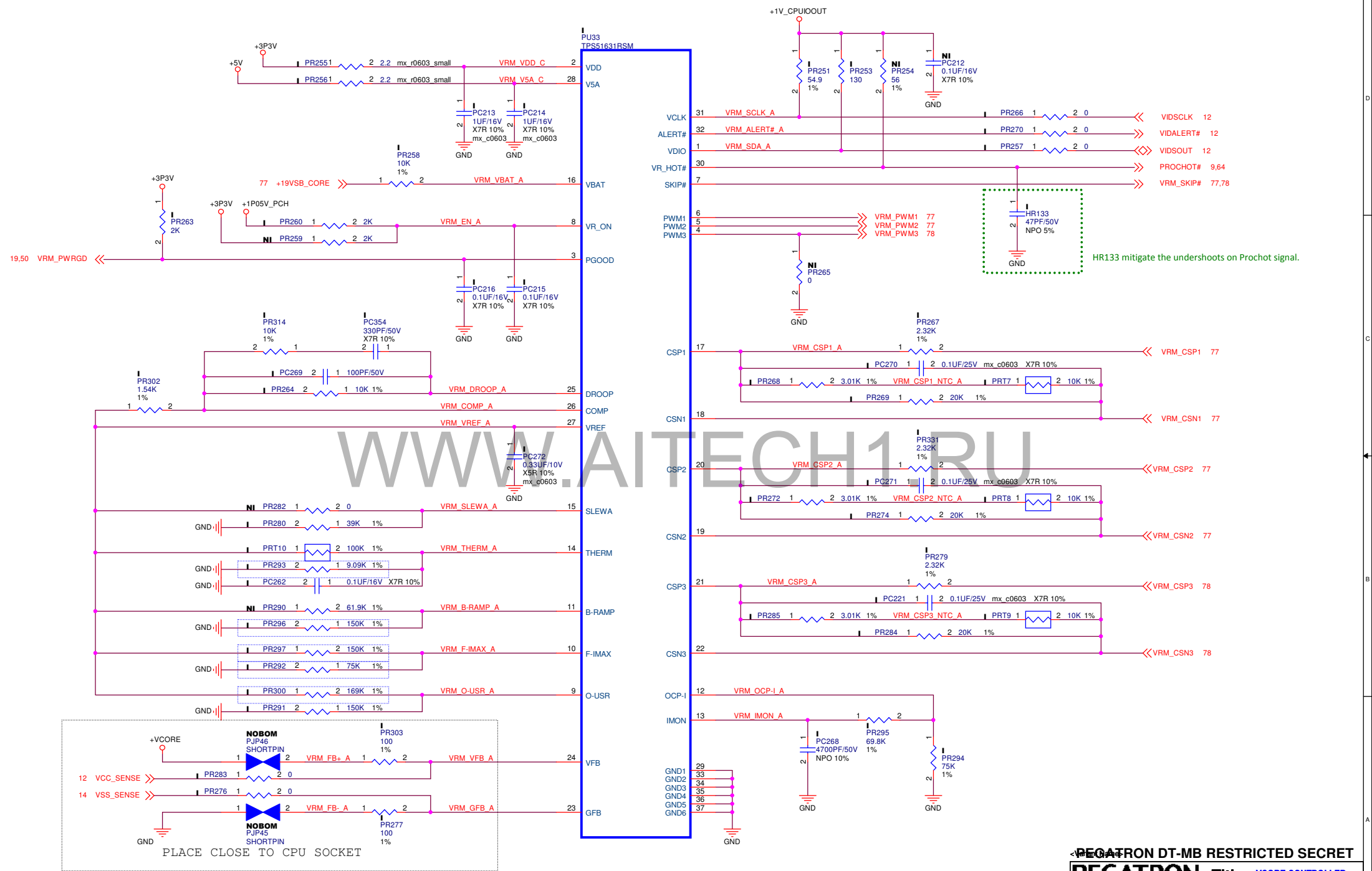
Fsw=300KHz@5V
lin=3.963A
lin,rms5.67A
delta l=3.72A
ESR=55mOhm
OCP=17.92A@MAX*1.4 times
H/S: 0.763W(BSC0909NS *1)
L/S: 1.681W (BSC0909NS *1)

Fsw=355KHz@3V
lin=1.7011A
lin,rms3.16A
delta l=2.33A
ESR=55mOhm
OCP=11.655A@MAX*1.4 times
H/S: 0.347W(BSC0909NS *1)
L/S: 1.082W (BSC0909NS *1)

(+3P3VSB+3P3VA+3P3V+3P3V_GPU+1P8V_MXM)
(3.72+0.023+2.552+0.09+1.94=8.325A)

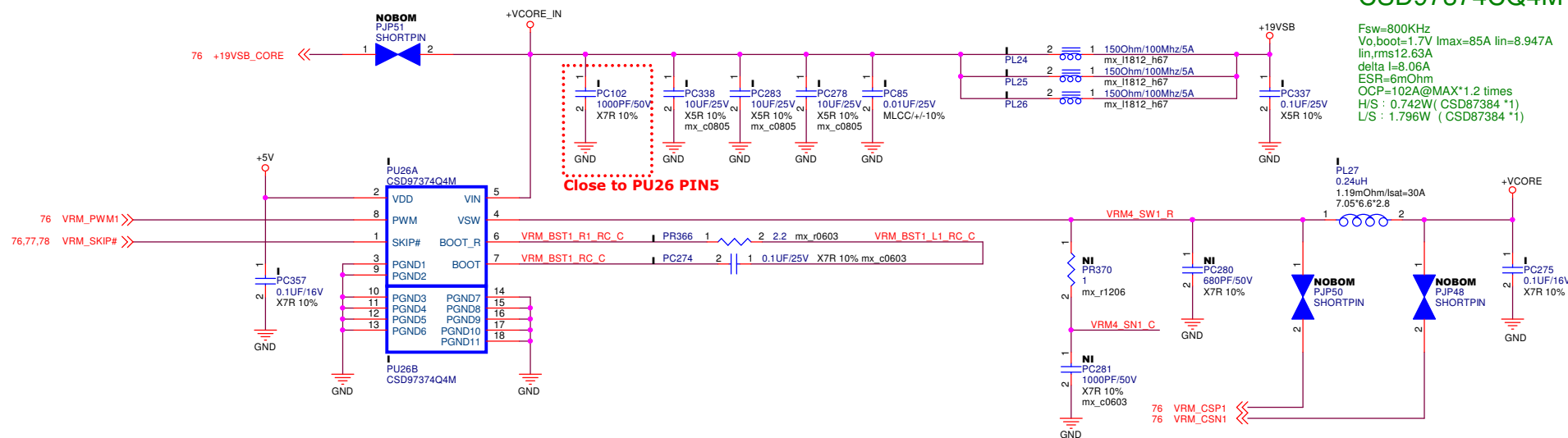
+5VSB(Imax=0.5A)
Imax=12.8A/TDC=6.3364A
(0.351A+5VA+5V_DUAL+5V)
(0.5+0.001+9.3+3=12.8A)

+3P3VSB(I=3.72A)
Imax=8.325A/TDC=5.8275A

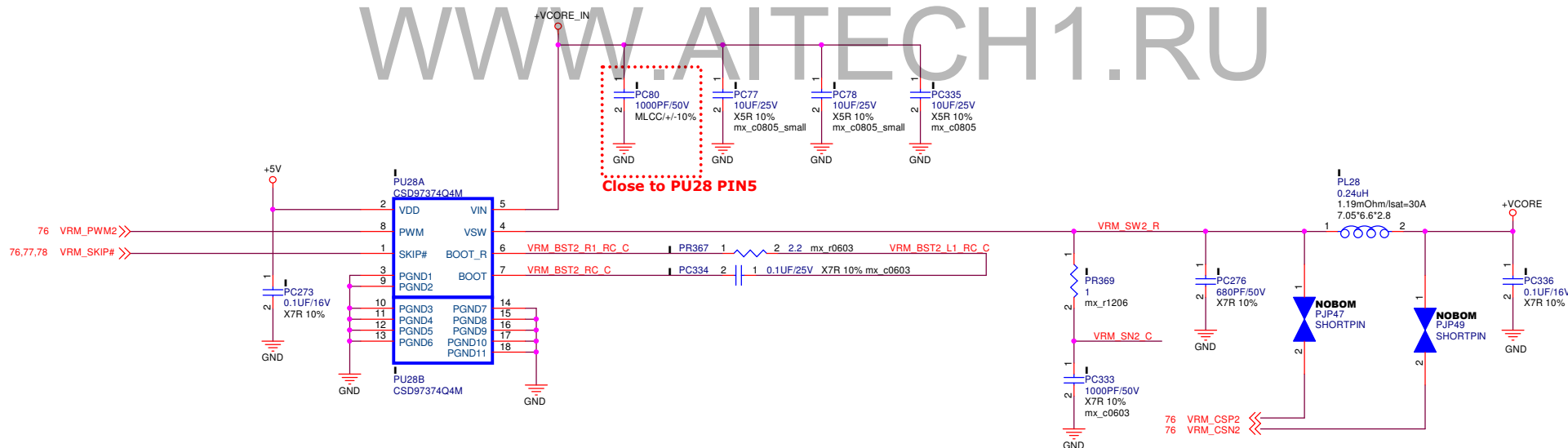


+Vcore
 $I_{max}=85A/TDC=27A$
 $F_{sw}=800KHz$
 CSD97374CQ4M * 3

$F_{sw}=800KHz$
 $V_o,boot=1.7V$ $I_{max}=85A$ $lin=8.947A$
 $lin_{rms}=12.63A$
 $\Delta I=8.06A$
 $ESR=6m\Omega$
 $OCP=102A@MAX*1.2$ times
 $H/S : 0.742W (CSD87384 *1)$
 $L/S : 1.796W (CSD87384 *1)$



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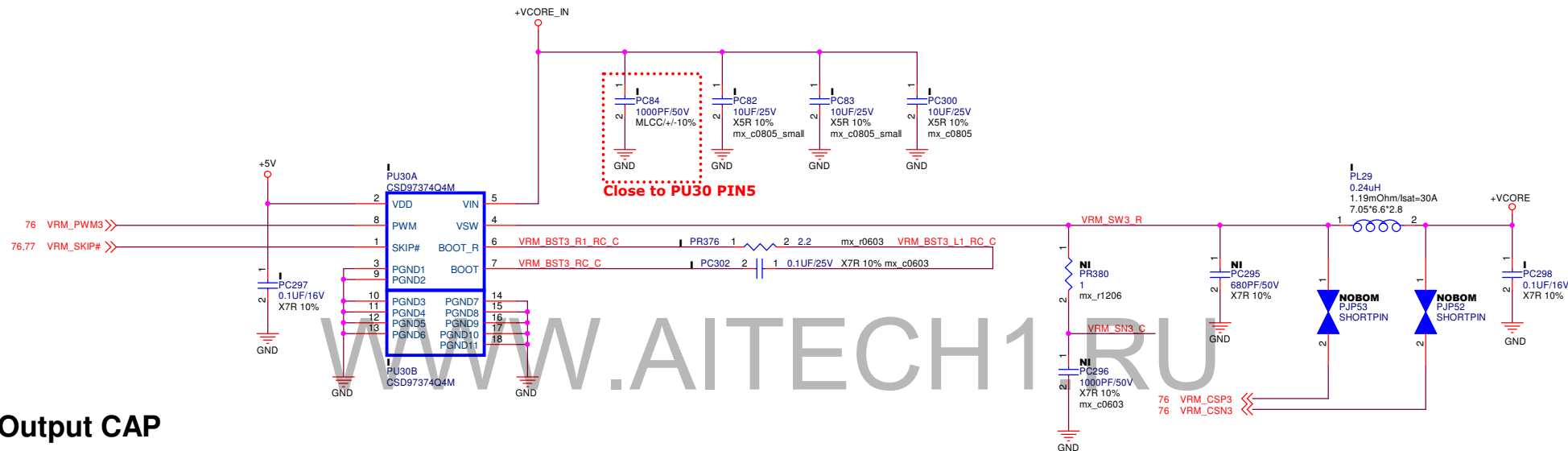
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **Vcore DRIVER**

Pegatron Corp. Engineer: **Stonko_Chen**

Size A3 Project Name **IMPLP-MS** Rev A00

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Output CAP

330 UF * 2

22 UF * 30 pcs

had checked with vendor

put in page12

PEGATRON DT-MB RESTRICTED SECRET

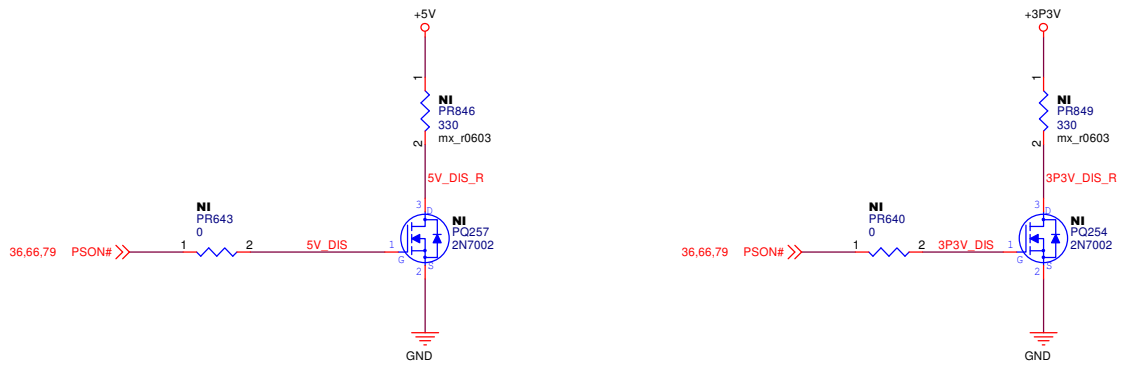
PEGATRON Title : V CORE OUTPUT CAP

Pegatron Corp. Engineer: Stonko_Chen

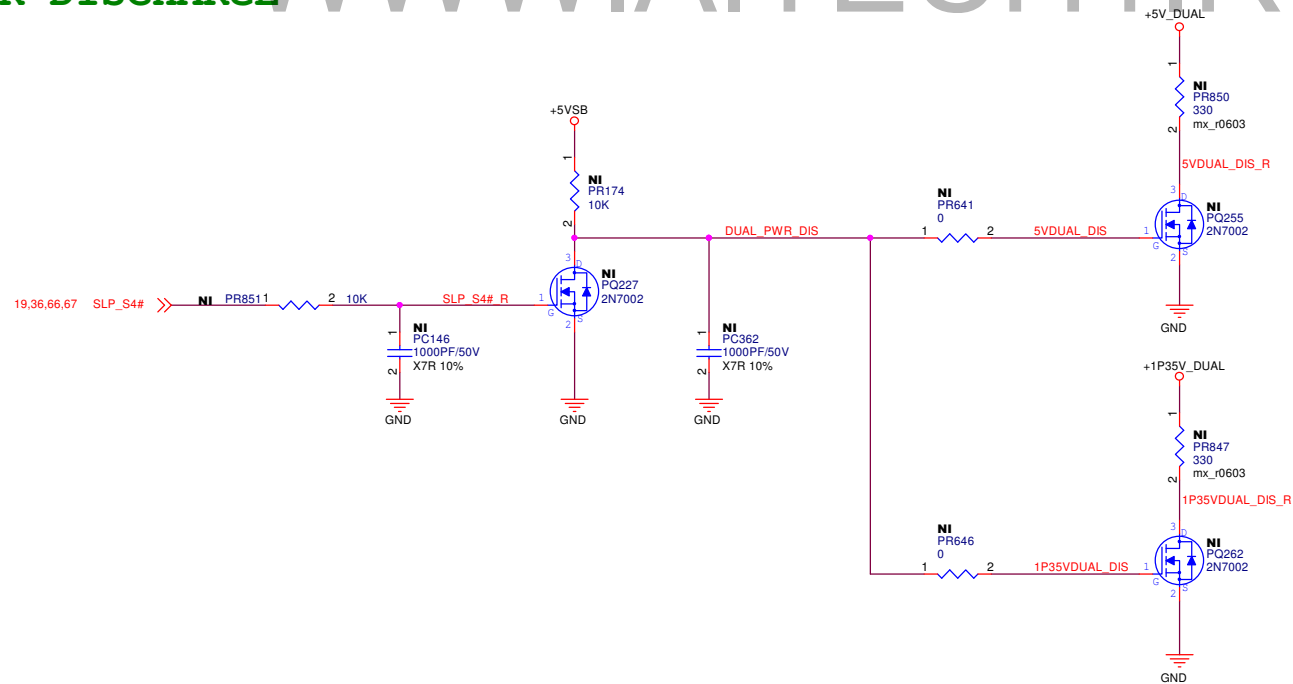
Size A3 Project Name IMPLP-MS Rev A00

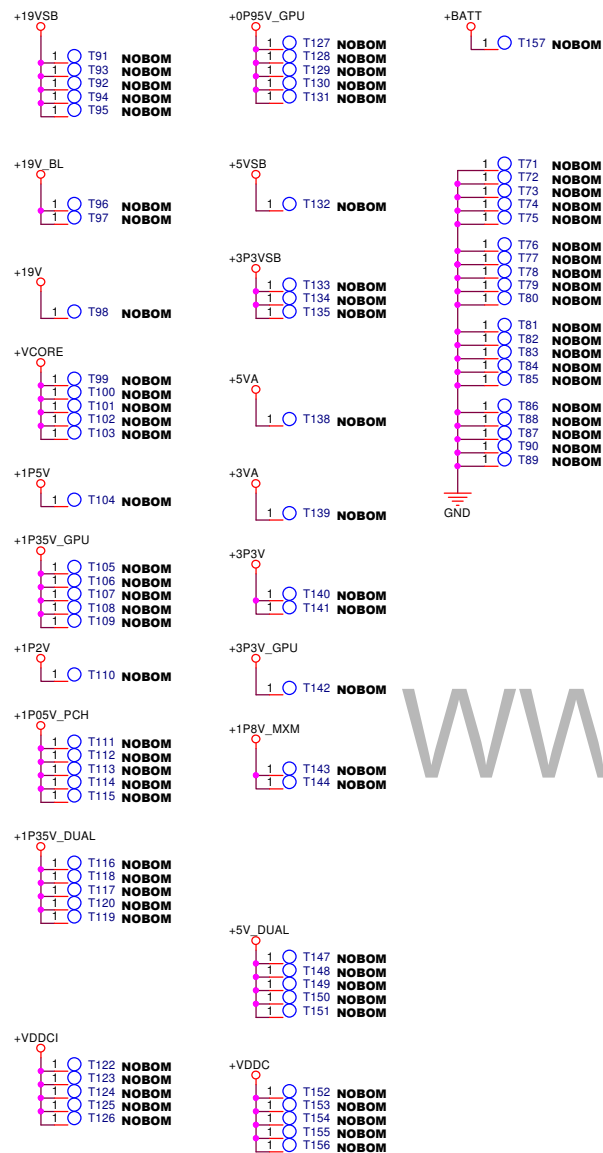
Date: Thursday, June 27, 2013 Sheet 78 of 83

MAIN POWER DISCHARGE



DUAL POWER DISCHARGE





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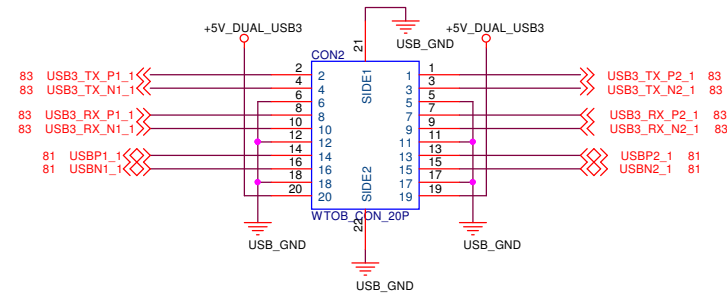
<PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : TEST POINT

Pegatron Corp. Engineer: **Stonko Chen**

Size	Project Name	Rev
A3	IMPLP-MS	A00

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